



# High Speed PWM Controller

## FEATURES

- Compatible with Voltage or Current-Mode Topologies
- Practical Operation @ Switching Frequencies to 1.0MHz
- 50ns Propagation Delay to Output
- High Current Totem Pole Output (1.5A peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start/Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V  $\pm$ 1%)

## DESCRIPTION

The UC1823 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage-mode systems with the capability for input voltage feed-forward.

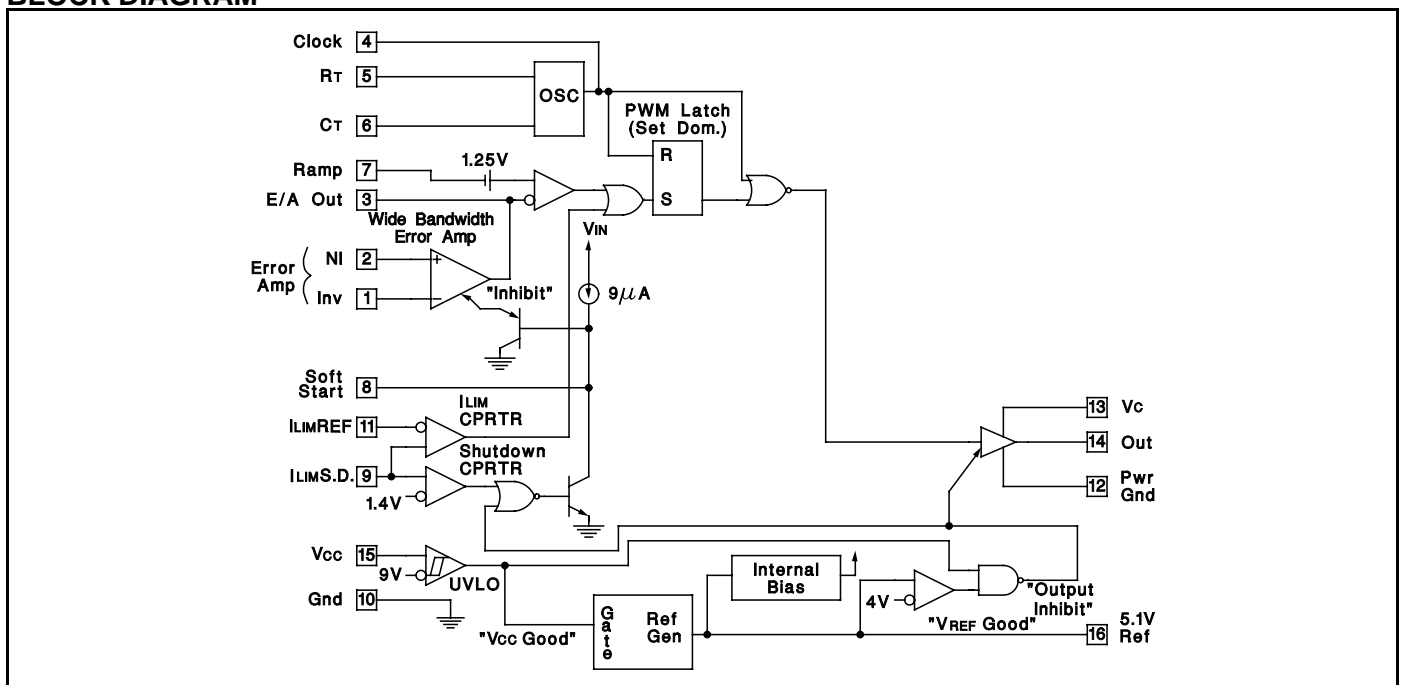
Protection circuitry includes a current limit comparator, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at the output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the output is high impedance. The current limit reference (pin 11) is a DC input voltage to the current limit comparator. Consult specifications for details.

These devices feature a totem pole output designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is defined as a high level.

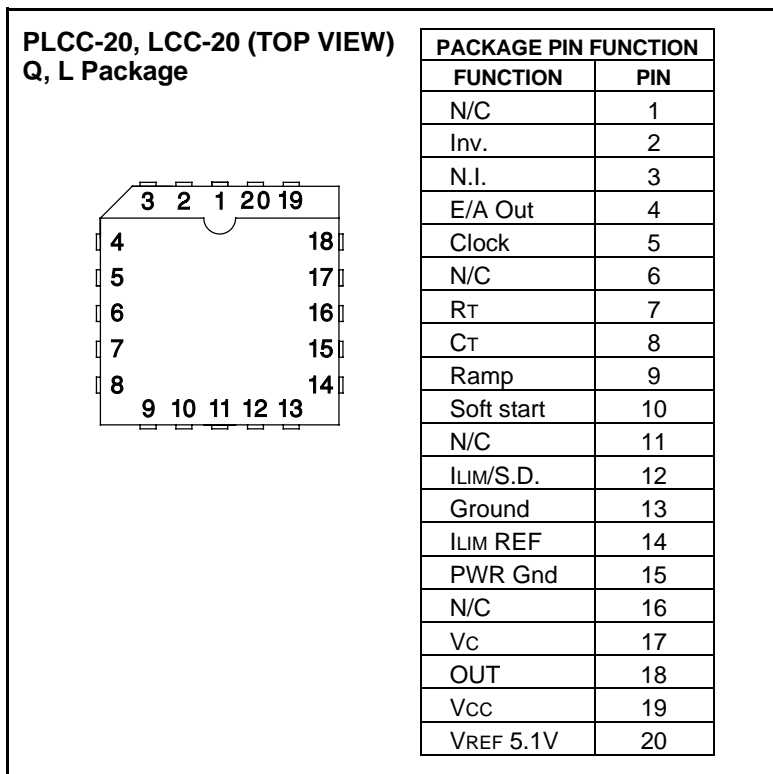
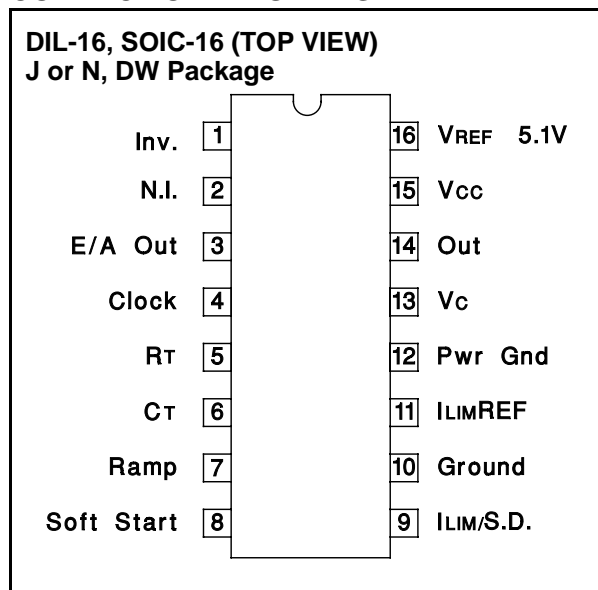
## ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13) .....	30V	Oscillator Charging Current (Pin 5) .....	-5mA
Output Current, Source or Sink (Pin14)		Power Dissipation at $T_A = 60^\circ\text{C}$ .....	1W
DC .....	0.5A	Storage Temperature Range .....	-65°C to +150°C
Pulse (0.5 $\mu$ s) .....	2.0A	Lead Temperature (Soldering, 10 seconds) .....	300°C
Analog Inputs (Pins 1, 2, 7, 8, 9, 11) .....	-0.3V to +6V	Note: All voltages are with respect to ground, Pin 10.	
Clock Output Current (Pin 4) .....	-5mA	Currents are positive into the specified terminal.	
Error Amplifier Output Current (Pin 3) .....	5mA	Consult Packaging Section of Databook for thermal	
Soft Start Sink Current (Pin 8) .....	20mA	limitations and considerations of packages.	

## BLOCK DIAGRAM



CONNECTION DIAGRAMS



**ELECTRICAL CHARACTERISTICS:** Unless otherwise noted, these specifications apply for  $R_T = 3.65k$ ,  $C_T = 1nF$ ,  $V_{CC} = 15V$ ,  $0^\circ C < T_A < +70^\circ C$  for the UC3823,  $-25^\circ C < T_A < +85^\circ C$  for the UC2823, and  $-55^\circ C < T_A < +125^\circ C$  for the UC1823,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Reference Section</b>								
Output Voltage	$T_J = 25^\circ C$ , $I_o = 1mA$	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	$10 < V_{CC} < 30V$		2	20		2	20	mV
Load Regulation	$1 < I_o < 10mA$		5	20		5	20	mV
Temperature Stability*	$T_{MIN} < T_A < T_{MAX}$		0.2	0.4		0.2	0.4	mV/ $^\circ C$
Total Output Variation*	Line, Load, Temp.	5.00		5.20	4.95		5.25	
Output Noise Voltage*	$10Hz < f < 10kHz$		50			50		$\mu V$
Long Term Stability*	$T_J = 125^\circ C$ , 1000 hrs.		5	25		5	25	mV
Short Circuit Current	$V_{REF} = 0V$	-15	-50	-100	-15	-50	-100	mA
<b>Oscillator Section</b>								
Initial Accuracy*	$T_J = 25^\circ C$	360	400	440	360	400	440	kHz
Voltage Stability*	$10 < V_{CC} < 30V$		0.2	2		0.2	2	%
Temperature Stability*	$T_{MIN} < T_A < T_{MAX}$		5			5		%
Total Variation*	Line, Temp.	340		460	340		460	kHz
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V

\* These parameters are guaranteed by design but not 100% tested in production.

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PARAMETER	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Error Amplifier Section</b>								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	$\mu A$
Input Offset Current			0.1	1		0.1	1	$\mu A$
Open Loop Gain	$1 < V_O < 4V$	60	95		60	95		dB
CMRR	$1.5 < V_{CM} < 5.5V$	75	95		75	95		dB
PSRR	$10 < V_{CC} < 30V$	85	110		85	110		dB
Output Sink Current	$V_{PIN 3} = 1V$	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN 3} = 4V$	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN 3} = -0.5mA$	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN 3} = 1mA$	0	0.5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/ $\mu S$
<b>PWM Comparator Section</b>								
Pin 7 Bias Current	$V_{PIN 7} = 0V$		-1	-5		-1	-5	$\mu A$
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero D.C. Threshold	$V_{PIN 7} = 0V$	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
<b>Soft-Start Section</b>								
Charge Current	$V_{PIN 8} = 0.5V$	3	9	20	3	9	20	$\mu A$
Discharge Current	$V_{PIN 8} = 1V$	1			1			mA
<b>Current Limit/Shutdown Section</b>								
Pin 9 Bias Current	$0 < V_{PIN 9} < 4V$			$\pm 10$			$\pm 10$	$\mu A$
Current Limit Offset	$V_{PIN 11} = 1.1V$			15			15	mV
Current Limit Common Mode Range ( $V_{PIN 11}$ )		1.0		1.25	1.0		1.25	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output*			50	80		50	80	ns
<b>Output Section</b>								
Output Low Level	$I_{OUT} = 20mA$		0.25	0.40		0.25	0.40	V
	$I_{OUT} = 200mA$		1.2	2.2		1.2	2.2	V
Output High Level	$I_{OUT} = -20mA$	13.0	13.5		13.0	13.5		V
	$I_{OUT} = -200mA$	12.0	13.0		12.0	13.0		V
Collector Leakage	$V_C = 30V$		100	500		100	500	$\mu A$
Rise/Fall Time*	$C_L = 1nF$		30	60		30	60	ns
<b>Under-Voltage Lockout Section</b>								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
<b>Supply Current</b>								
Start Up Current	$V_{CC} = 8V$		1.1	2.5		1.1	2.5	mA
$I_{CC}$	$V_{PIN 1}, V_{PIN 7}, V_{PIN 9} = 0V, V_{PIN 2} = 1V$		22	33		22	33	mA

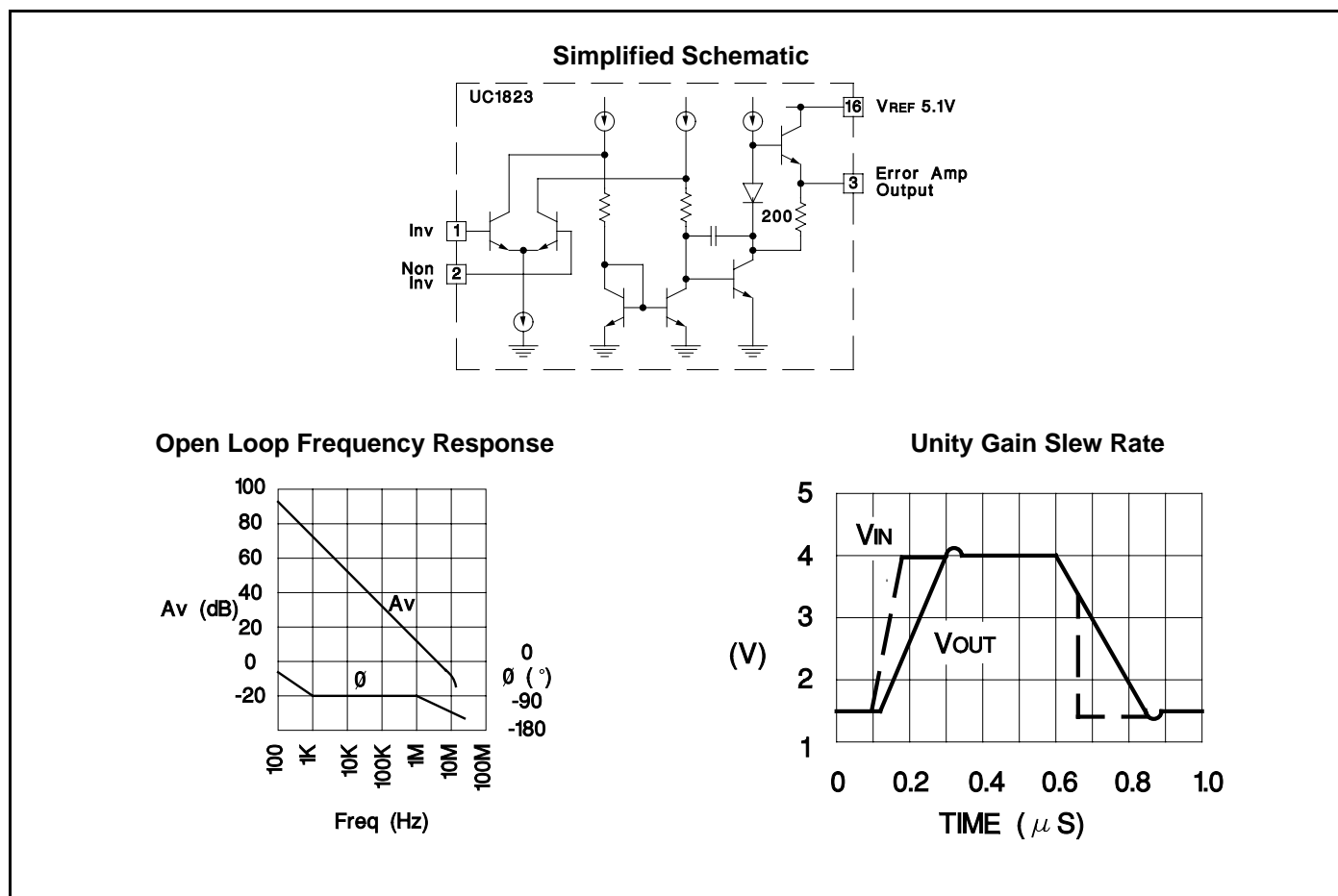
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## UC1823 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

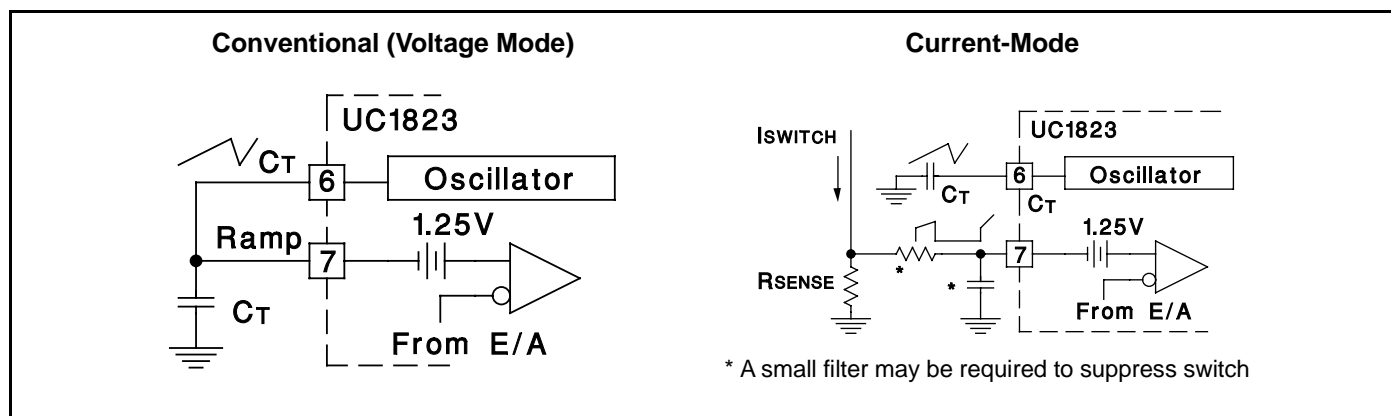
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1823, follow these rules. 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFET. Don't allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve

this purpose. 3) Bypass VCC, VC, and VREF. Use 0.1 $\mu$ F monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, CT, like a bypass capacitor.

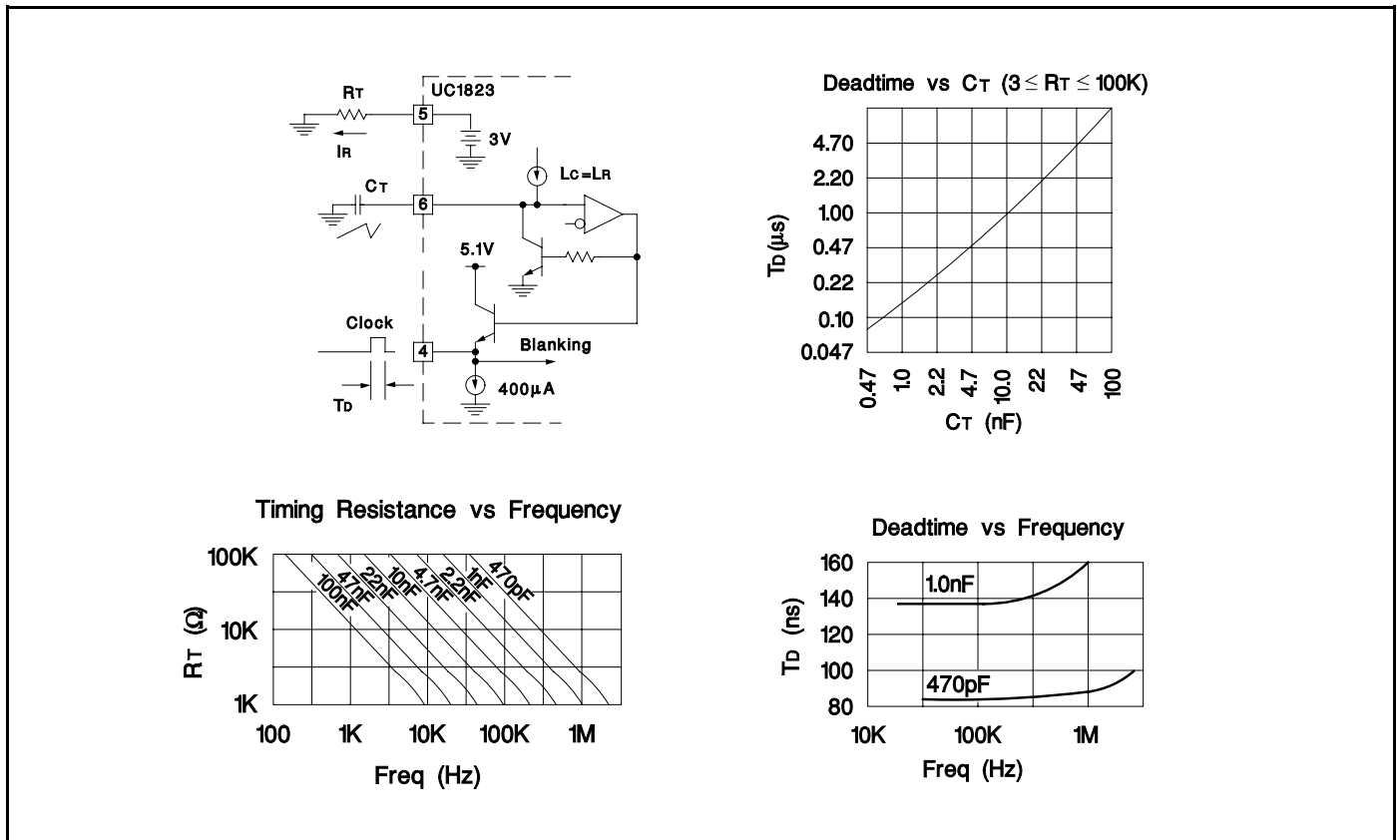
## ERROR AMPLIFIER CIRCUIT



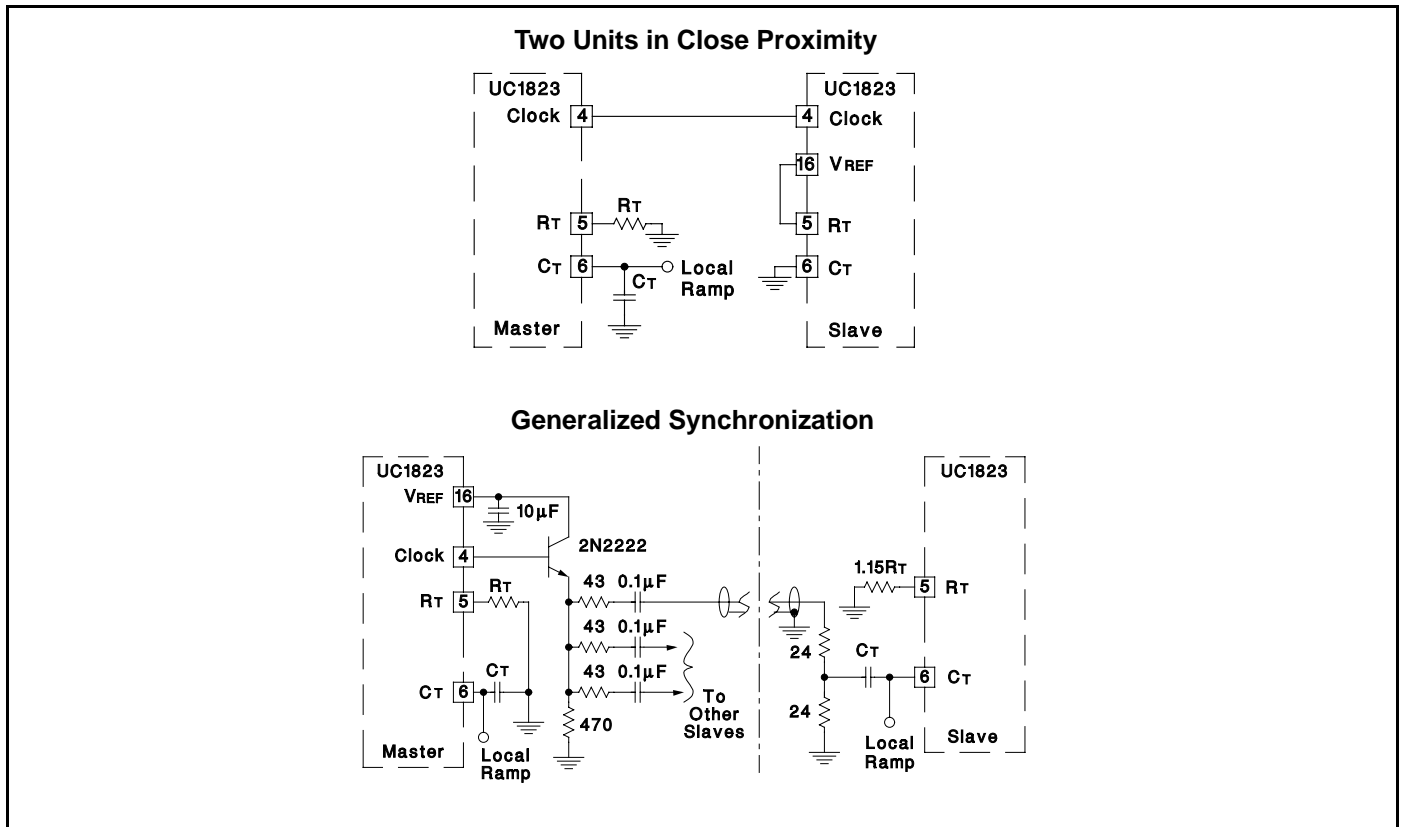
## PWM APPLICATIONS



OSCILLATOR CIRCUIT

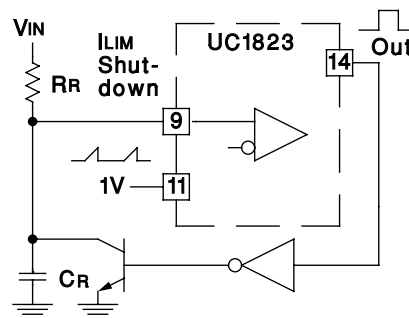


SYNCHRONIZED OPERATION



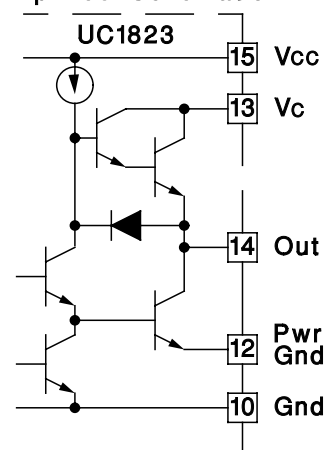
### CONSTANT VOLT-SECOND CLAMP CIRCUIT

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components,  $R_T$  and  $C_R$  are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the inverter must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

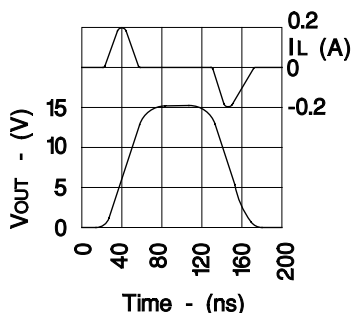


### OUTPUT SECTION

Simplified Schematic



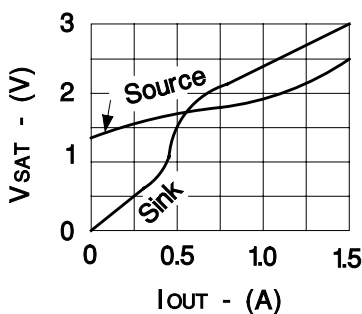
Rise/Fall Time ( $C_L=1nF$ )



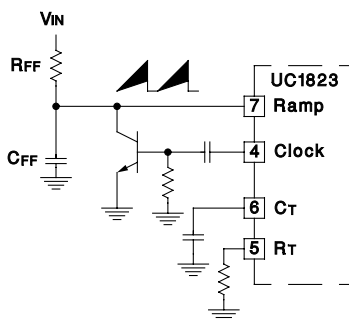
Rise/Fall Time ( $C_L=10nF$ )



Saturation Curves



### FEED FORWARD TECHNIQUE FOR OFF-LINE VOLTAGE MODE APPLICATION



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-89905012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-8990501EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1823J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1823J883B	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1823L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
UC1823L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
UC2823DW	ACTIVE	SOIC	DW	16	40	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC2823DWTR	ACTIVE	SOIC	DW	16	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC2823N	ACTIVE	PDIP	N	16	25	TBD	CU NIPDAU	Level-NA-NA-NA
UC2823Q	ACTIVE	PLCC	FN	20	46	TBD	Call TI	Level-2-220C-1 YEAR
UC2823QTR	ACTIVE	PLCC	FN	20	1000	TBD	Call TI	Level-2-220C-1 YEAR
UC3823DW	ACTIVE	SOIC	DW	16	40	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC3823DWTR	ACTIVE	SOIC	DW	16	2000	TBD	CU NIPDAU	Level-2-220C-1 YEAR
UC3823DWTRG4	PREVIEW	SOIC	DW	16	2000	TBD	Call TI	Call TI
UC3823J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	Level-NC-NC-NC
UC3823N	ACTIVE	PDIP	N	16	25	TBD	CU NIPDAU	Level-NA-NA-NA
UC3823Q	ACTIVE	PLCC	FN	20	46	TBD	Call TI	Level-2-220C-1 YEAR
UC3823QTR	ACTIVE	PLCC	FN	20	1000	TBD	Call TI	Level-2-220C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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