LT1070 Design Manual

Carl Nelson

INTRODUCTION

Three terminal monolithic linear voltage regulators appeared almost 20 years ago, and were almost immediately successful for a variety of reasons. In particular, there were relatively few engineers capable of designing a good linear voltage regulator. The new devices were also easy to use, and inexpensive. In currently popular parlance they were "expert systems," containing a good deal of their designer's knowledge in silicon form. Because of these advantages, the regulators quickly eclipsed discrete and earlier monolithic building blocks and dominated the market.

More recently, there has been increasing interest in switching-based regulators. Switching regulators, with their high efficiency and small size, are increasingly desirable as overall package sizes have shrunk. Unfortunately, switching regulators are also one of the most difficult linear circuits to design. Mysterious modes, sudden failures, peculiar regulation characteristics and just plain explosions are common occurrences during the design of a switching regulator.

Most switching regulator ICs are building blocks. Many discrete components are required, and substantial expertise is assumed on the part of the user. Some newer devices include the power switch on the die, but still require a significant amount of engineering to apply. Finally, there has been a notable lack of comprehensive and practical application literature support from manufacturers.

These considerations are reminiscent of the state of linear regulator design when the first three terminal monolithic regulators appeared. Given this historical lesson, the LT®1070 five terminal switching regulator has been designed for ease of use and economy. It does not require the user to be well-schooled in switching regulator design, and is versatile enough to be used in all the popular switching regulator configurations. To obtain maximum user benefit, a significant applications effort has been associated with this part. This note covers both ancillary tutorial material as well as direct operating considerations for the part. It is intended to be used "as required." For those in a mission-oriented hurry, much of the discussion can be ignored, and breadboards constructed with a high probability of success. The more academically inclined reader may choose to peruse the material more carefully. Either approach is valid and the note is intended to satisfy both.

— Jim Williams

TABLE OF CONTENTS

PREFACE

Smaller Versions of the LT1070

Since this application note was written, several new versions of the LT1070 have been developed. The LT1071 and LT1072 are identical to the LT1070 except for switch current ratings, 2.5A and 1.25A, respectively. Designs which result in lower switch currents can take advantage of the cost savings of these smaller chips. Design equations for the LT1071 and LT1072 are identical to the LT1070 with the following exceptions:

Peak Switch Current (I_P)	= 5A	LT1070
	= 2.5A	LT1071
	= 1.25A	LT1072
Switch "On" Resistance (R)	≈ 0.2Ω	LT1070
	≈ 0.4Ω	LT1071
	≈ 0.8Ω	LT1072
V_C Pin to Switch Current Transconductance	≈ 8A/V	LT1070
	≈ 4A/V	LT1071
	≈ 2A/V	LT1072

Also available in the 2nd quarter of 1989 will be 100kHz versions of the LT1070/LT1071/LT1072.

Inductance Calculations

Feedback from readers of AN19 shows that there is confusion about the use of ΔI to calculate inductance values. ΔI is the *change* in inductor or primary current during switch "on" time, and the suggested value is approximately 20% of the peak current rating of the LT1070 switch (5A), or in some cases, 20% of the average inductor current. This 20% rule-of-thumb is designed to give near maximum output power for a given switch current rating. If maximum output power is not needed, much smaller inductors/transformers may be used by allowing ΔI to increase. The design approach is to calculate peak inductor/switch current (I_P) using the formulas provided in AN19, with L = ∞.

Then compare this current to the peak switch current. The difference is the "room" allowable for ΔI;

$$\Delta I_{MAX} = 2(I_{SWITCH(PEAK)} - I_P)$$

This formula assumes continuous mode operation. If ΔI, as calculated by this formula, exceeds I_P, it may be possible to go to discontinuous mode operation, with further reductions in inductance. Discontinuous mode requires higher switch currents and not all the AN19 topologies show design equations for this mode, but it should definitely be considered for very low output powers or where inductor/transformer size is critical. All topologies work well in discontinuous mode with the exception of fully isolated flyback. Drawbacks of discontinuous mode include higher output ripple and slightly lower efficiency.

Example 1: Negative buck converter with V_{IN} = –24V, V_{OUT} = –5V and I_{OUT} = 1.5A,

$$I_P(\text{Equation 37}) = I_{OUT} + \frac{(V_{IN} - V_{OUT})(V_{OUT})}{2 \bullet V_{IN} \bullet f \bullet (L \approx \infty)} = I_{OUT} = 1.5A$$

$$\Delta I_{MAX} = 2(I_{SW} - I_P) = 2(5 - 1.5) = 7A \text{ (LT1070)}$$
$$= 2(2.5 - 1.5) = 2A \text{ 9(LT1071)}$$
$$= 2(1.25 - 1.5) \text{ - N.A. (LT1072)}$$

The LT1072 is too small ($I_P > I_{SW}$), so select the LT1071, which yields a maximum ΔI of 2A. A conservative value of actual ΔI is selected at 1A. This allows room for efficiency losses and variations in component values. Using Equation 37:

$$L = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{V_{IN}(\Delta I) \bullet f} = \frac{(24 - 5)(5)}{24(1) \bullet 40k} = 99\mu H$$

Example 2: Flyback converter with V_{IN} = 6V, V_{OUT} = ±15V at 35mA and 5V at 0.2A, N = 0.4 (primary to 5V secondary). For calculations, the entire output power of 2.05W is referred to the 5V secondary, yielding one value for N(0.4), V_{OUT} (5V) and I_{OUT} = 0.41A.

Using Equation 79:

$$I_P = \frac{I_{OUT}}{E}\left(\frac{V_{OUT}}{V_{IN}} + N\right) + \frac{(V_{IN})(V_{OUT})}{2 \bullet f(V_{OUT} + N\,V_{IN})(L = \infty)}$$

$$= \frac{0.41A}{0.75}\left(\frac{5V}{6V} + 0.4\right) = 0.674A$$

The LT1072 is large enough to handle this current, yielding;

$$\Delta I_{MAX} = 2(1.25A - 0.674A) = 1.15A$$

Using a conservative value of 0.7A for ΔI (note that this is 56% of the 1.25A Max LT1072 switch current, not 20%), and Equation 77, yields:

$$L = \frac{(V_{IN})(V_{OUT})}{\Delta I \bullet f(V_{OUT} + N\,V_{IN})} = \frac{(6)(5)}{(0.7)(40k)(5 + 0.4 \bullet 6)} = 145\mu H$$

Protecting the Magnetics

A second problem for LT1070 designers has been protection of the magnetics under overload or short-circuit conditions. Physical size restraints often require inductors or transformers which are not specified to handle the full current limit values of the LT1070. This problem can be handled in several ways.

1. Use an LT1071 or LT1072 if full load current requirements allow it.
2. Take advantage of the fact that the LT1070 current limit *drops* at higher temperatures. The worst-case current limit values shown on the old data sheets allow for both temperature extremes with one specification. New data sheets will specify a maximum of 10A for the LT1070, 5A for the LT1071 and 2.5A for the LT1072 at temperatures of 25°C or higher. Be aware that the temperature dependence of current limit has been improved considerably on the LT1070 since the original data sheet was printed. The old value was greater than –0.3%/°C, while the new figure is under –0.1%/°C. The current limit graphs on the new data sheets reflect this improved characteristic.
3. Reconsider the necessity of limiting the inductor/transformer current to the manufacturers' specification. Maximum current ratings in many cases are determined by core saturation considerations. Allowing the core to saturate does *not* harm the core. Core or winding damage occurs only if temperatures rise so far that material properties are permanently altered. Core saturation used to be considered a "fatal" condition for conventional switchers because currents would "run away" and destroy switches or diodes. The LT1070 limits current on an instantaneous cycle-by-cycle basis, preventing current "run away" even with grossly overdriven cores. The major consideration then is the heating effect of the winding current (I^2R). Under short-circuit conditions, winding currents in inductors are nearly constant at the current limit value of the LT1070. Transformer *secondary* winding currents are nearly constant at 1/N times the LT1070 current limit. This assumes that the core is not heavily saturated. If the core saturates significantly below the current limit values, RMS winding current will be significantly l*ower* than the current limit. The best way to resolve this complex situation is to actually measure core/winding temperature with a thermocouple under overload conditions. The thermocouple should be "buried" as deeply as possible in the windings and/or core to reflect peak temperatures. The magnetic and electric fields generated by the switching may affect the thermocouple meter. If this occurs, simply check the temperature periodically by turning off power. Consult with the magnetics manufacturer to determine peak allowable temperatures, with permanent damage as the criteria, not performance specifications. The major failure mode is winding shorts caused by insulation melting. High temperature insulation is available from most manufacturers.

New Switch Current Specification

The LT1070 was specified at 5A peak switch current, for duty cycles of 50% or less. At higher duty cycles the peak current was limited to 4A. This abrupt change in specification at 50% duty cycle was bothersome because many designs operate near 50% duty cycle and require maximum possible output power. To solve this problem, switch current limit on new data sheets will be specified as a linearly decreasing function, from 5A at 50% duty cycle to 4A at 80% duty cycle. The LT1071 and LT1072 will also be specified this way.

High Supply Voltages

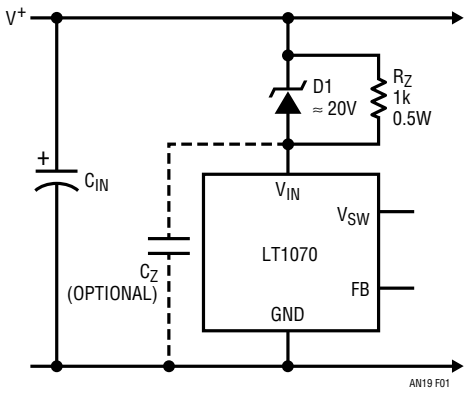
It has become apparent that many applications for the LT1070 have maximum input voltages which exceed 40V. The straightforward approach is to use the "HV" devices that are specified at 60V, but in some cases the standard part can be used at lower cost simply by dropping supply voltage with a Zener diode as shown. The LT1070 supply pin (V_{IN}) requires only a few volts to operate, so in most cases the unregulated input voltage range is not compromised with this Zener. Zener dissipation can be calculated from $I_Z \approx 6mA + I_{SW}(0.0015 + DC/40)$:

I_{SW} = LT1070 average switch current during "on" time
DC = duty cycle

For I_{SW} = 4A, DC = 30%; I_Z = 42mA

A 20V Zener would dissipate (20)(42) = 0.84W. Note that this power would be dissipated anyway in the LT1070, so no loss in efficiency occurs. The resistor, R_Z, is necessary for start-up. Without it, a latch-off condition exists where the V_{IN} pin sits more than 16V negative with respect to the switch pin. If the LT1070 is not switching and the FB pin is below 0.5V, the LT1070 is in the "isolated flyback" mode where it is trying to regulate the V_{IN} -to-V_{SW} voltage. When this voltage exceeds 16V, the regulator thinks it should reduce duty cycle to zero, resulting in a permanent "no-switching" state. R_Z forces the V_{IN} pin to rise enough to initiate start-up. The user need not be concerned that the V_{IN}-to-ground pin voltage exceeds 40V during this state because R_Z is too large to allow harmful currents to flow.

Some attention needs to be paid to C_Z. The LT1070 is very tolerant of noise and ripple on the V_{IN} pin, but C_Z may be necessary in some applications. The problem is that D1 must charge C_Z when power is applied. If power comes up very rapidly, D1 might exceed its one cycle surge rating.



Discontinuous "Oscillations" (Ringing)

Many customers have called about oscillations occurring on the switch pin during a portion of the switch "off" time. These are not oscillations. They are a damped ringing caused by the transition to a zero-current state in the inductor or transformer primary. At light loads, or with low inductance values, inductor current will drop to zero during switch off time. This causes the inductor voltage to collapse toward zero. In doing so, however, energy is transferred back to the inductor from the parasitic capacitance of the switch, inductor, and catch diode. The inductor and capacitance form a parallel resonant tank which "rings." This ringing is not harmful as long as its peak amplitude does not result in a negative voltage on the switch pin. It can be damped, if desired, by paralleling the inductor/primary with a series R/C damper, typically 100Ω to 1kΩ, and 500pF to 5000pF. Typical undamped ringing frequency is 100kHz to 1MHz.

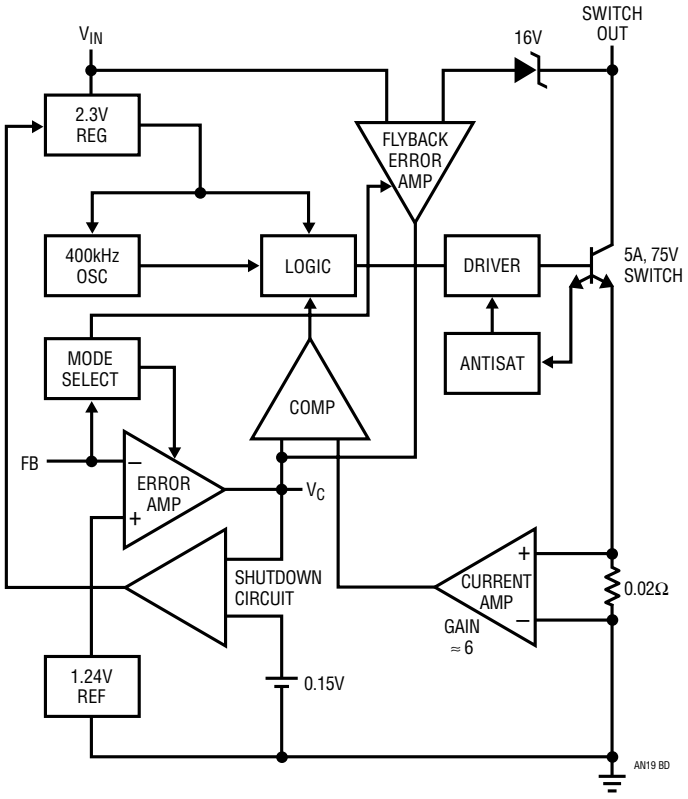
LT1070 OPERATION

The LT1070 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the Block Diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage-sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at midfrequencies in the energy storage inductor. This greatly simplifies closed-loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1070. This low dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive antisat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the LT1070 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1070 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2V (high output current). The error amplifiers are current output (g_m) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 50µA supply current for shutdown circuitry biasing.

Block Diagram



PIN FUNCTIONS

Input Supply (V_{IN})

The LT1070 is designed to operate with input voltages from 3V to 40V (standard) or 60V (HV units). Supply current is essentially flat over this range at about 6mA (with zero output current). With increasing switch current, the supply current (during switch on-time) increases at a rate approximately 1/40 of switch current, corresponding to a forced h_{FE} of 40 for the switch.

Undervoltage lockout is incorporated on the LT1070 by sensing saturation of the lateral PNP pass transistor which drives an internal 2.3V regulator. A remote collector on this transistor conducts current and locks out the switch for input voltages below 2.5V. No hysteresis is used to maximize the useful range of input voltage. Operating the regulator right at the 2.5V threshold may result in a "burping" action as the LT1070 turns on and off in response to wobbles in input voltage, but this will not harm the device. External undervoltage lockout can be added if it is desirable to raise the threshold voltage. The circuit shown in Figure 1 is one example of how to implement this.

The threshold of this circuit is approximately V_Z + 1.5V. Below that voltage, D2 pulls the V_C pin low to shut off the regulator.

Ground Pin

The ground pin (case) of the LT1070 is important because it acts as both the negative sense point for the internal error amplifier and as the high current path for the 5A switch. This is not normally good design practice, but was necessary in a 5-pin package configuration. *To avoid degradation of load regulation, Kelvin connections should be made to the ground pin*. This is done on the TO-3 package by tying one end of the package to power ground and the other end to the feedback divider resistor (analog ground). This is illustrated in Figure 2.

For best load regulation, the resistance in the switch current path must be kept low. 0.01Ω of wire resistance creates 50mV drop at 5A switch current. This is a 1% change in a 5V output, and actually causes the output to *increase* with increasing load current.

With the TO-220 package, (Figure 3) connect the feedback resistor directly to the ground pin with a separate wire if no case connection is made. The case can be used as a second ground pin if desired.

Avoid long wire runs to the ground pin to minimize load regulation effects and inductive voltages created by the high di/dt switch current. A ground plane will keep EMI to a minimum

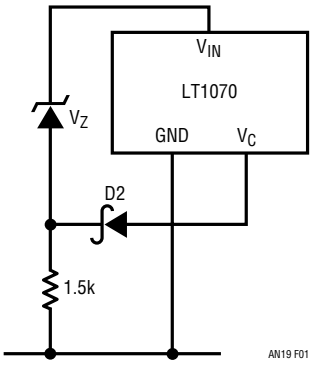


Figure 1. External Undervoltage Lockout

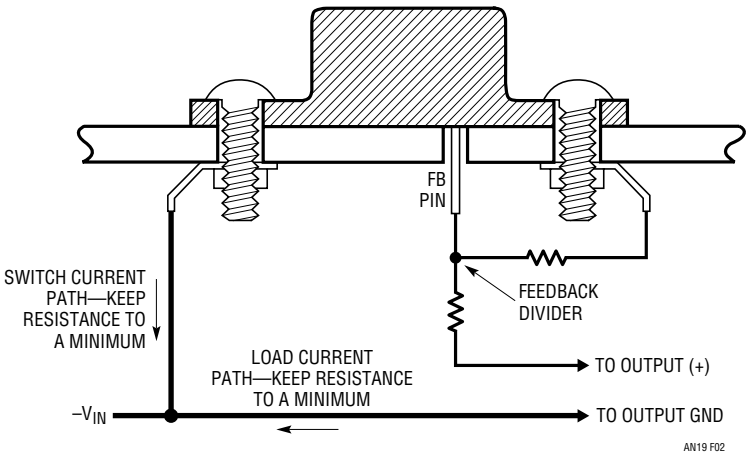


Figure 2

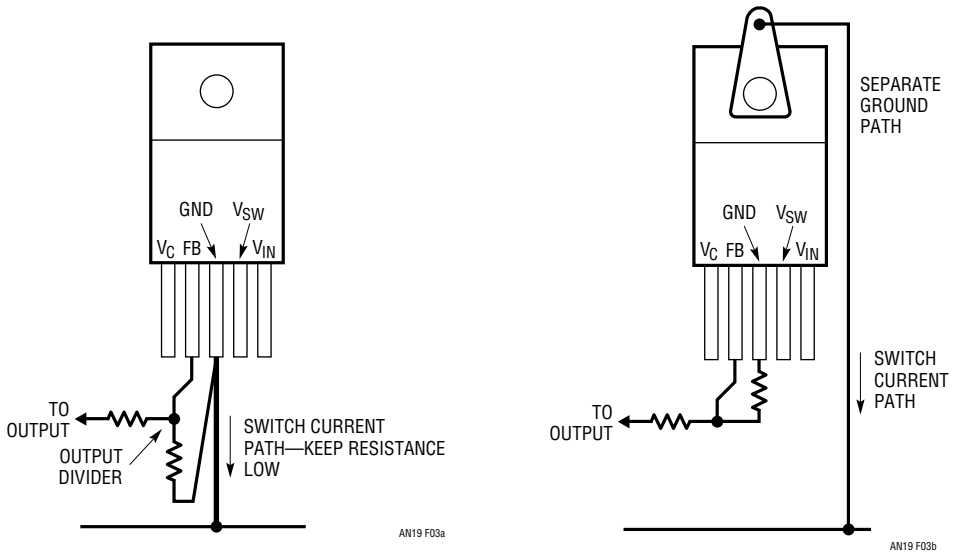


Figure 3

Feedback Pin

The feedback pin is the inverting input to a single stage error amplifier. The noninverting input to this amplifier is internally tied to a 1.244V reference as shown in Figure 4.

Input bias current of the amplifier is typically 350nA with the output of the amplifier in its linear region. The amplifier is a g_m type, meaning that it has high output impedance with controlled voltage-to-current gain ($g_m \approx 4400\mu$mhos). DC voltage gain with no load is ≈ 800.

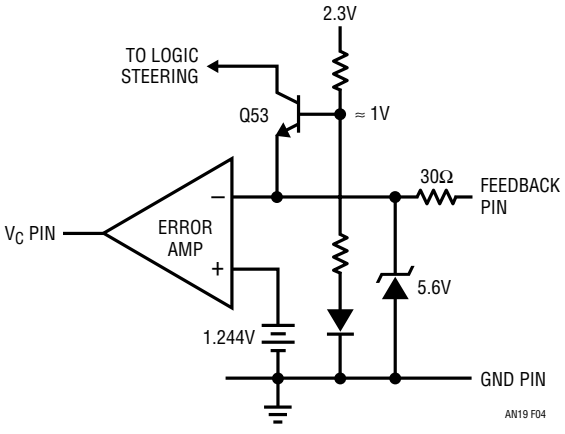


Figure 4

The feedback pin has a second function; it is used to program the LT1070 for normal or flyback-regulated operation (see description of block diagram). In Figure 4, Q53 is biased with a base voltage approximately 1V. This clamps the feedback pin to about 0.4V when current is drawn out of the pin. A current of ≈10μA or higher through Q53 forces the regulator to switch from normal operation to flyback mode, but this threshold current can vary from 3μA to 30μA. *The LT1070 is in flyback mode during normal start-up until the feedback pin rises above 0.45V.* The resistor divider used to set output voltage will draw current out of the feedback pin until the output voltage is up to about 33% of its regulated value.

If it is desired to run the LT1070 in the *fully isolated* flyback mode, a single resistor is tied from the feedback pin to ground. The feedback pin then sits at a voltage of ≈ 0.4V for R = 8.2k. The actual voltage depends on resistor value since the feedback pin has about 200Ω output impedance in this mode. 500μA in the resistor will drop the feedback pin voltage from 0.4V to 0.3V. Minimum current through the resistor to guarantee flyback operation is 50μA. Actual resistor value is chosen to fine-trim flyback regulated voltage. (See discussion of isolated flyback mode operation and graphs of feedback pin characteristics.)

An internal 30Ω resistor and 5.6V Zener protect the feedback pin from overvoltage stress. Maximum transient voltage is ±15V. This high transient condition most commonly occurs during fast fall time output shorts if a feedforward capacitor is used around the feedback divider. If a feedforward capacitor is used for DC output voltages greater than 15V, a resistor equal to V_{OUT}/20mA should be used between the divider node and the feedback pin as shown in Figure 5.

Keep in mind when using the LT1070 that the feedback pin reference voltage is referred to the ground pin of the regulator, and the ground pin can have switch currents exceeding 5A. Any resistance in the ground pin connection will degrade load regulation. Best regulation is obtained by tying the grounded end of the feedback divider directly to the ground pin of the LT1070, as a separate connection from the power ground. This limits output voltage errors to just the drop across the ground pin resistance instead of multiplying it by the feedback divider ratio. See discussion of ground pin.

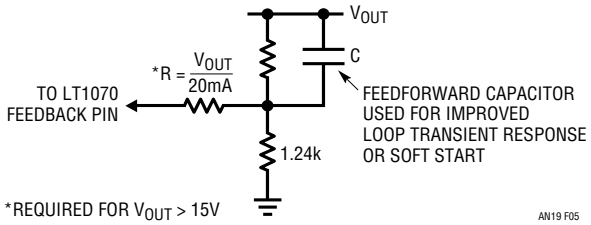


Figure 5

Compensation Pin (V_C)

The V_C pin is used for frequency compensation, current limiting, soft start and shutdown. It is the output of the error amplifier and the input of the current comparator. The error amplifier circuit is shown in Figure 6.

Q57 and Q58 form a differential input stage whose collector currents are inverted and multiplied times four by Q55 and Q56. Q55 current is further inverted by Q60 and Q61 to generate a current fed balanced output which can swing from the 2.3V rail down to a clamp level of ≈0.4V as set by

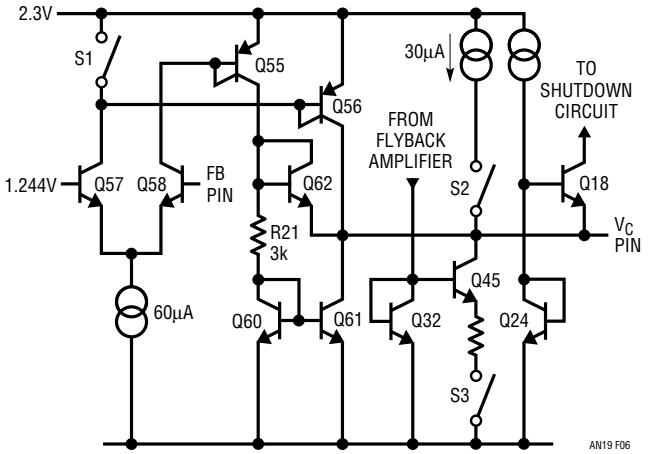


Figure 6. Error Amplifier

R21 and Q62. The 60µA tail current of the input transistors sets the g_m of the error amplifier at 4400µmhos. Voltage gain with no load is limited by transistor output impedance at ≈800. Maximum source and sink current is ≈220µA.

The voltage on the V_C pin determines the current level at which the output switch will turn off. For V_C voltage below 0.9V (at 25°C), the output switch will be totally off (duty cycle = 0). Above 0.9V, the switch will turn on at each oscillator cycle, then turn off when switch current reaches a trip level set by V_C voltage. This trip level is zero at V_C = 0.9V, and increases to about 9A when V_C reaches its upper clamp level of 2V. These numbers are based on a duty cycle of 10%. Above 10%, switch turn-off is a function of both switch current *and* time. The time dependence is caused by a small ramp fed into the current amplifier input. This ramp starts at ≈40% duty cycle, and is the source of the bend in the V_C vs duty cycle graph shown in Figure 7. This ramp is used to prevent a phenomenon peculiar to "current mode" switching regulators known as *subharmonic oscillation*. See section on Subharmonic Oscillations for further details.

A second amplifier output is also tied to the V_C pin. This "flyback mode" amplifier is turned on only when current is drawn *out* of the feedback pin. This condition occurs during start-up in the normal mode until the feedback divider has raised the voltage at the feedback pin above 0.45V.

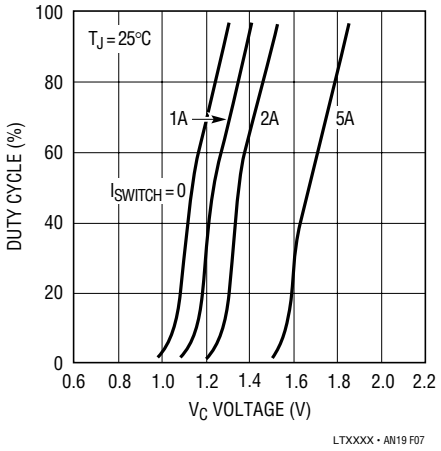


Figure 7. Duty Cycle vs V_C Voltage

It is a permanent condition when the LT1070 is programmed for isolated flyback mode by tying a single resistor from the feedback pin to ground.

In the isolated flyback mode, S1 is closed and the feedback pin is low, totally disabling the main amplifier. S2 and S3 are turned on only during the "off" state of the output power transistor and then, only after a 1.5µs delay following output transistor turn-off. This prevents transient flyback spikes from causing poor regulation. S2 current is fixed at 30µA. S3 current can rise to a maximum of ≈70µA, allowing the V_C pin to source 30µA and sink 40µA in the flyback mode. g_m of the flyback amplifier is typically 300µmho.

When the V_C pin is externally pulled below 0.15V, a shutdown circuit is activated. Q24 and Q18 perform this function. Q24 is a special "high V_{BE}" diode whose forward voltage is about 150mV higher than Q18 V_{BE}. Pulling current out of Q18 activates shutdown and turn off all internal regulator functions except for a 50µA to 100µA trickle current needed to bias Q18 and Q24. See characteristic curves for details of the V/I properties of the V_C pin in shutdown.

Loop frequency compensation can be performed with an RC network connected from the V_C pin to ground. An optional compensation is to connect the RC network between the V_C pin and the feedback pin. See Loop Frequency Compensation section.

Output Pin

The V_{SW} pin of the LT1070 is the collector of the internal NPN power switch. This NPN has a typical on-resistance of 0.15Ω and a breakdown voltage (BV_{CBO}) of 85V. Very fast switching times and high efficiency are obtained by using a special driver loop which automatically adapts base drive current to the minimum required to keep the switch in a quasi-saturation state. This loop is shown in Figure 8.

Q104 is the power switch. Its base is driven by Q101, whose collector is returned to V_{IN}. Q101 is turned on and off by Q102. In parallel with Q102 is a second, larger transistor (Q103) which pulls high reverse base current out of Q104 for rapid switch turn-off. The key element in the loop is the extra emitter on Q104. This emitter carries no current when Q104 collector is high (unsaturated). In this condition, the driver, Q101, can deliver very high base drive to the switch for fast turn-on. When the switch saturates, the extra emitter acts as a collector and pulls base current away from the driver. This linear feedback loop servos itself to keep the switch just at the edge of saturation. Very low switch currents result in near-zero driver current, and high switch currents automatically increase driver current as necessary. The ratio of switch current to driver current is approximately 40:1. This ratio is determined by the sizing of the extra emitter and the value of I_1. The quasi-saturation state of the switch permits rapid turn-off without the need for reverse base-emitter voltage drive.

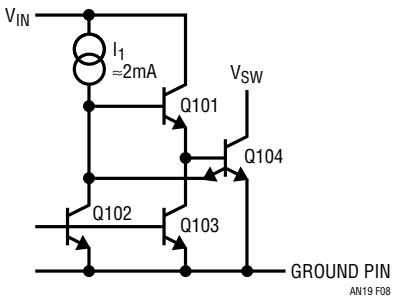


Figure 8

Also tied to the V_{SW} pin is the input circuitry for the flyback mode error amplifier as shown in Figure 9. This circuitry draws no current from the V_{SW} pin when the switch pin is *less* than 16V above V_{IN} because the diodes block current. When V_{SW} is more than 16V above V_{IN}, ≈500µA is drawn out of the switch pin because the reference diodes (D1 and D2) and Q10 turn on. This 500µA current level is set by the ratio of collector areas on the 2-collector lateral PNP Q10 and the value of I_2. Q9 is reverse biased in this state. The 16V transition point sets the flyback mode reference voltage. The flyback reference voltage can be increased above 16V by drawing additional current through R1 via Q52. The amplitude of this current is determined by the size of the resistor tied to the feedback pin. See discussion in Isolated Flyback Mode Operation.

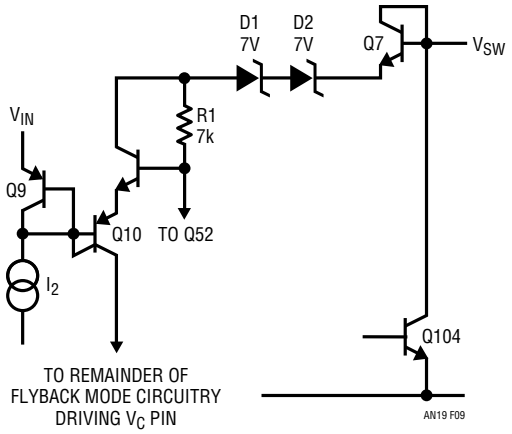


Figure 9

BASIC SWITCHING REGULATOR TOPOLOGIES

There are many possible switching regulator configurations, or "topologies." In any particular regulator requirement, the possible choices are narrowed somewhat by constraints of polarity, voltage ratio, and fault conditions (simple boost regulators cannot be current limited), but this may still leave the designer with several choices. To convert 28V to 5V, for instance, the list of possible topologies includes buck, flyback, forward and current boosted buck. The following discussion of topologies is limited to those which can be realized with the LT1070, but this covers nearly all the low to medium power DC/DC conversion requirements.

Buck Converter

Figure 10a shows the basic buck topology. S1 and S2 open and close alternately so that the voltage applied to L1 is either V_{IN} or zero. DC output voltage is then the average voltage applied to L1. If t_1 is the time S1 is closed, and t_2 is the time it is open, V_{OUT} is equal to:

$$V_{OUT} = V_{IN}\frac{t_1}{t_1 + t_2} = (V_{IN})(DC) \quad (1)$$

where, by convention, duty cycle (DC) is defined as the ratio of t_1 to $t_1 + t_2$;

$$DC = \frac{t_1}{t_1 + t_2} \quad (2)$$

Note that the definition of duty cycle allows only for values between 0 and 1. The formula for V_{OUT} therefore shows a basic property of buck converters; the *output voltage is always less than the input voltage*.

This simple formula also tells much about switching regulators in general. The most important point is what is *not* in the equation, *and that includes L1, C1, frequency and load current. To a first approximation, the output voltage of a switching regulator depends only on the duty cycle of the switching network and input voltage*. This is a very important point which must be kept firmly in mind when analyzing switching regulators.

Diodes may be used to replace switches when unidirectional current flow exists. In Figures 10b and 10c, single-switch buck regulators are shown with diodes used to replace S2. Diodes cause some loss in efficiency, but simplify the design and reduce cost. Notice that when S1 is closed, D1 is reverse biased (off) and that when S1 opens, the current flow through L1 forces the diode to become forward biased (on). This duplicates the alternate switching action of two switches. There is an exception to this condition, however. If the load current is low enough, the current through L1 will drop to zero sometime during S1 off-time. This is known as *discontinuous mode opera-*

tion. Buck regulators will be in discontinuous mode for any load current less than;

$$I_{OUT} \leq \frac{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{(2)(f)(L1)} \quad (3)$$

where f = switching frequency.

Discontinuous mode alters the original statement that output voltage depends only on input voltage and switch duty cycle because a third state of the switches now exists with diodes replacing S2; namely both switches off. Waveforms for voltage and current of S1, D1, L1, C1 and the input source are shown for both continuous and discontinuous modes of operation.

Normally it is not important to avoid discontinuous mode operation at light load currents. A possible exception to this would be when the "on" time of S1 cannot be reduced to a low enough value to prevent the lightly loaded output from drifting unregulated high. If this occurs, most switching regulators will begin "dropping cycles" wherein S1 does not turn on at all for one or more cycles. This mode of operation maintains control of the output, but the subharmonic frequencies generated may be unacceptable in certain situations.

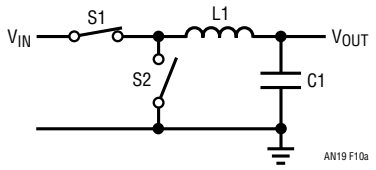
A general property of "perfect" switching regulators is that they do not dissipate power in the process of converting one voltage or current to another; in other words, they are 100% efficient. This is to be expected from an inspection of Figure 10a: *there are no components which dissipate power*, only switches, inductors and capacitors. The following formula can then be stated;

$$P_{OUT} = P_{IN} \text{ or, } (I_{OUT})(V_{OUT}) = (I_{IN})(V_{IN}) \quad (4)$$

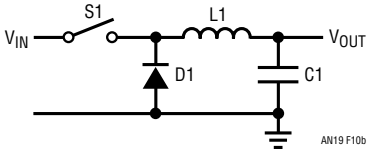
and

$$I_{IN} = I_{OUT}\left(\frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

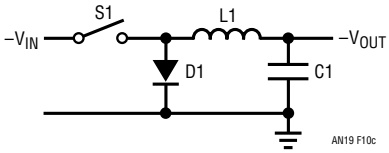
This shows that the *average current drawn by the input of a switching regulator can be much higher or lower than the load current*, depending on the ratio of output-to-input



a. Basic Topology



b. Positive Buck Using One Switch



c. Negative Buck Using One Switch

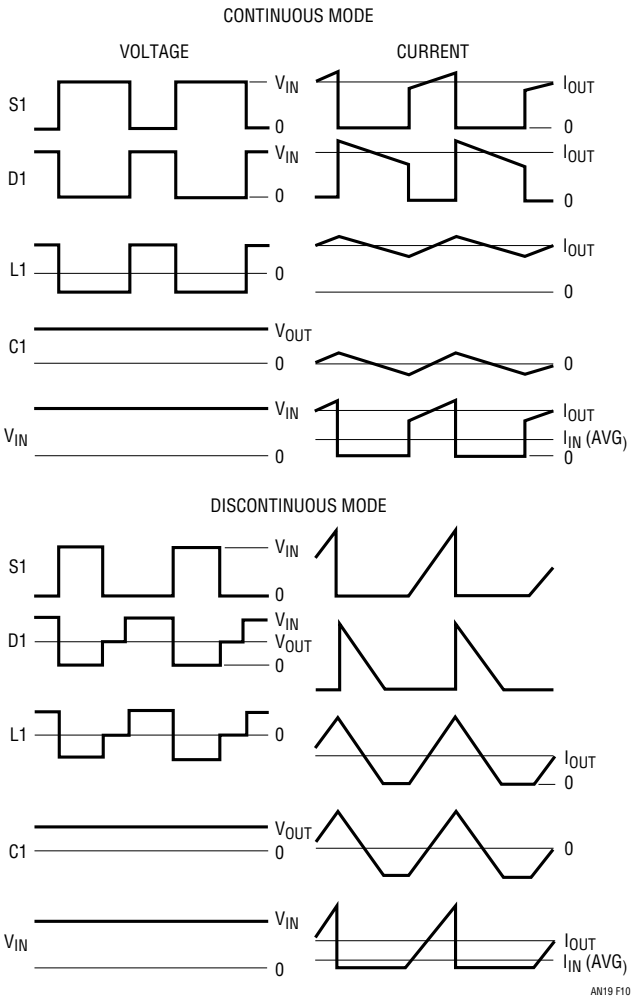


Figure 10. Buck Converter

voltage. If this simple fact is ignored, the designer may realize too late that his low voltage to high voltage converter will draw more current from the low voltage supply than it is capable of handling.

Boost Regulators

The basic boost regulator shown in Figure 11a has an output voltage given by;

$$V_{OUT} = \frac{V_{IN}}{1-DC} \text{(continuous mode)} \quad (6)$$

DC is duty cycle, the ratio of S1 "on" time to "off" time, assuming that S1 and S2 open and close alternately. Duty cycle can take on values only between 0 and 1; therefore, *the output voltage of a boost regulator is always higher than the input voltage*.

In Figure 11b, a diode has replaced S2 to realize a boost regulator with a single switch. The voltage and current waveforms for all the components including the source are shown, both for continuous and discontinuous mode. Note that the current drawn from the input and delivered in pulses to the load is significantly higher than the output load current. The amplitude of input current and peak switch and diode current is equal to;

$$I_P = I_{OUT}\frac{V_{OUT}}{V_{IN}} \text{(continuous mode)} \quad (7)$$

Average diode current is equal to I_{OUT} and *average* switch current is $I_{OUT}(V_{OUT} - V_{IN})/V_{IN}$, both of which are significantly less than peak current. *The switch, diode and output capacitor must be specified to handle the peak currents as well as average currents*. Discontinuous mode requires even higher ratios of switch current to output current.

One drawback of boost regulators is that they cannot be current limited for output shorts because the current steering diode, D1, makes a direct connection between input and output.

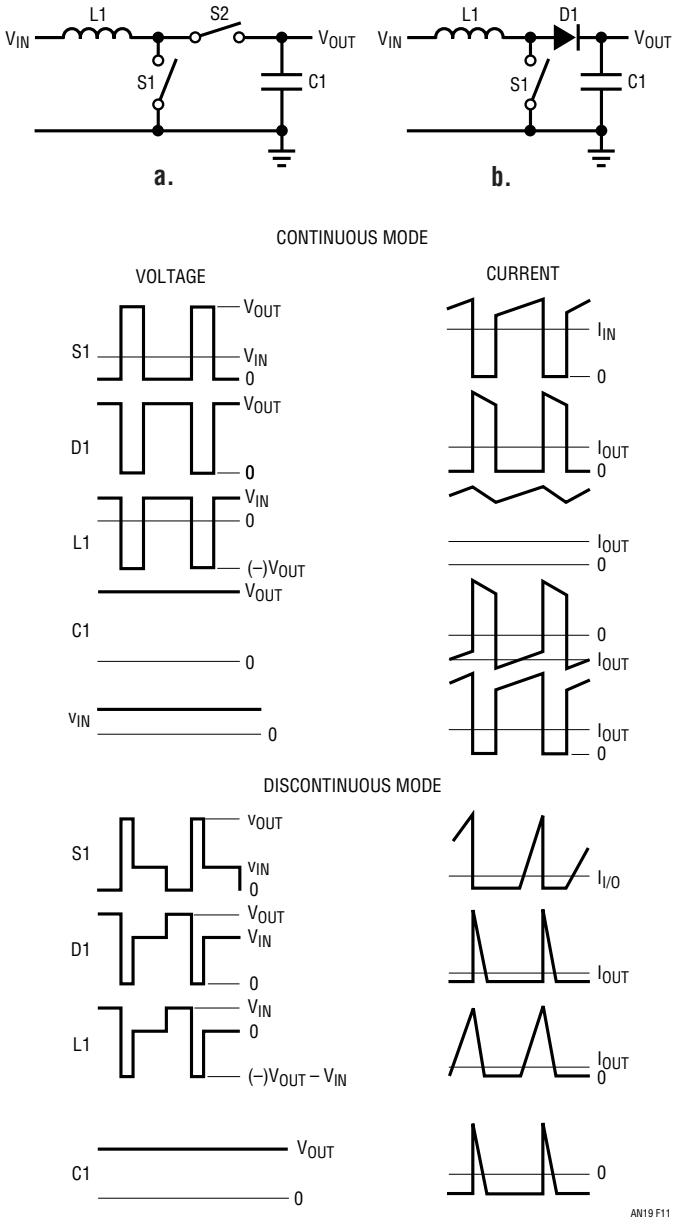


Figure 11. Boost Regulators

Combined Buck-Boost Regulator

Buck-boost regulators (Figure 12) are used to generate an output with the reverse polarity of the input. They look similar to a boost regulator except that the load is referred to the inductor side of the input instead of the switch side. Buck-boost regulators have an output voltage given by;

$$V_{OUT} = -V_{IN}\left(\frac{DC}{1-DC}\right) \quad (8)$$

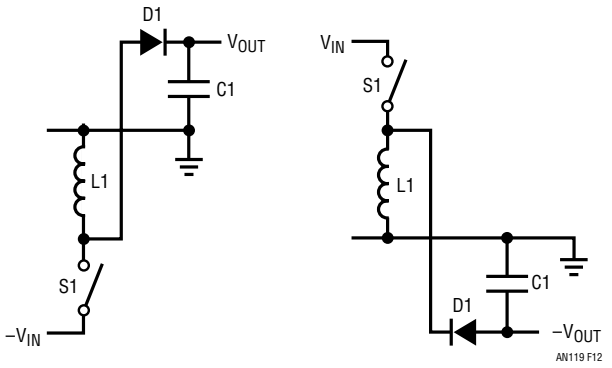


Figure 12. Inverting Topology

With duty cycle varying between 0 and 1, the output voltage can vary between zero and an infinitely high value. The current and voltage waveforms show that, like boost regulators, the peak switch, diode, and output capacitor currents can be significantly higher than output currents and these components must be sized accordingly.

$$I_{PEAK} = \frac{I_{OUT}}{1-DC} = I_{OUT}\frac{(V_{OUT}+V_{IN})}{V_{IN}}(\text{continuous mode}) \quad (9)$$

Maximum switch voltage is equal to the sum of input plus output voltage. The forward turn-on time of D1 is therefore very important in higher voltage applications to prevent additional switch stress.

'Cuk Converter

The 'Cuk converter in Figure 13 is named after Slobodan 'Cuk, a professor at Cal Tech. It is like a buck-boost converter in that input and output polarities are reversed, but it has the advantage of low ripple current at both input and output. The optimum topology version of the 'Cuk converter eliminates the disadvantage of needing two inductors by winding them both on the same core, with exact 1:1 turns ratio. With slight adjustments to L1 or L2, *either* input ripple current *or* output ripple current can be forced to zero. An impvoved version even exists which results in *both* ripple currents going to zero. This considerably eases the requirements on size and quality of input and output capacitors without requiring filters.

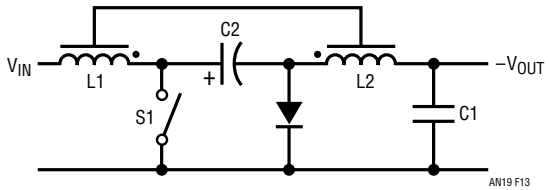


Figure 13. 'Cuk Converter

The switch must handle the *sum* of input and output current;

$$I_{PEAK}(S1) = I_{IN} + I_{OUT} = I_{OUT}\left(1+\frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

The ripple current in C2 is equal to I_{OUT}, so this capacitor must be large. It can be electrolytic, however, so physical size is not normally a problem.

Flyback Regulator

Flyback regulators (Figure 14) use a transformer to transfer energy from input to output. During S1 "on" time, energy builds up in the core due to increasing current in the primary winding. At this time, the polarity of the output winding is such that D1 is reverse biased. When S1 opens, the total stored energy is transferred to the secondary winding and current is delivered to the load. The turns ratio (N) of the transformer can be adjusted for optimum power transfer from input to output.

Peak switch current in a flyback regulator is equal to:

$$I_{PEAK}(S1) = \frac{I_{OUT}(N\,V_{IN}+V_{OUT})}{V_{IN}}(\text{continuous mode})$$

Notice that peak switch current can be reduced to a minimum by using a very small value for N. This has two

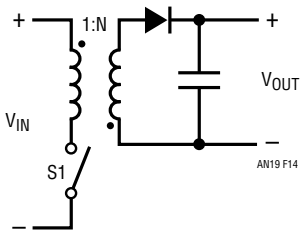


Figure 14. Flyback Converter

negative consequences however; the switch voltage and diode current become very large during switch off time. For a given maximum switch voltage, optimum power transfer occurs at $V_{IN} = 1/2V_{MAX}$.

Both input ripple current *and* output ripple current are high in a flyback regulator, but this disadvantage is more than offset in many cases by the ability to achieve current or voltage gain and the inherent isolation afforded by the transformer. Output voltage is given by:

$$V_{OUT} = V_{IN} \bullet N \bullet \frac{DC}{1-DC} \quad (11)$$

With any value of N, a duty cycle between 0 and 1 can be found which generates the required output. *Flyback regulators can have an output voltage which is higher or lower than the input voltage.*

A disadvantage of flyback regulators is the high energy which must be stored in the transformer in the form of DC current in the windings. This requires larger cores than would be necessary with pure AC in the windings.

Forward Converter

A forward converter (Figure 15) avoids the problem of large stored energy in the transformer core. It does this, however, at the expense of an extra winding on the transformer, two more diodes, and an additional output filter inductor. Power is transferred from input to the load through D1 during switch "on" time. When the switch turns "off," D1 reverse biases and L1 current flows through D2. Output voltage is equal to:

$$V_{OUT} = V_{IN} \bullet N \bullet DC \quad (12)$$

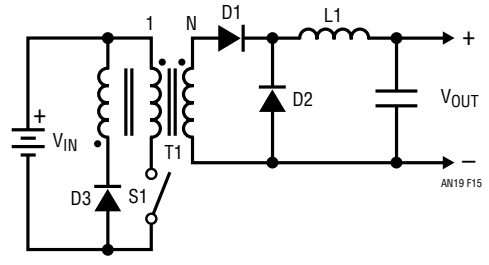


Figure 15. Forward Converter

The additional winding and D3 are required to define switch voltage during switch "off" time. Without this clamp, switch voltage would jump all the way to breakdown at the moment the switch is opened due to the magnetizing current flowing in the primary. This "reset" winding normally has a 1:1 turns ratio to the primary which limits switch duty cycle to 50% maximum. Above this duty cycle, switch current rises uncontrolled even with no load because the primary winding cannot maintain zero DC voltage. Reducing the number of turns on the reset winding will allow higher switch duty cycles at the expense of higher switch voltage.

Output voltage ripple of forward converters tends to be low because of L1, but input ripple current is high due to the low duty cycles normally used. A smaller core can be used for T1 compared to flyback regulators because there is no net DC current to saturate the core.

Current-Boosted Boost Converter

This topology in Figure 16 is an extension of the standard boost converter. A tapped inductor is used to decrease the switch current for a given load current. This allows higher load currents at the expense of higher switch voltage. The increase in maximum output power over a standard boost converter is equal to:

$$\frac{P_{OUT}}{P_{BOOST}} = \frac{(N+1)(V_{OUT})}{N(V_{OUT} - V_{IN}) + V_{OUT}} \quad (13)$$

Analysis of this equation shows that significant increases in power are possible when the input-output differential is low. Care must be used, however, to ensure that maximum switch voltage is not exceeded.

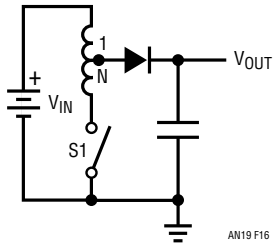


Figure 16. Current-Boosted Boost Converter

Current-Boosted Buck Converter

The current boosted buck converter in Figure 17 uses a transformer to increase output current above the maximum current rating of the switch. It accomplishes this at the expense of increased switch voltage during switch "off" time. The increase in maximum output current over a standard buck converter is equal to:

$$\frac{I_{OUT}}{I_{BUCK}} = \frac{V_{IN}}{V_{OUT} + N\left(V_{IN} - V_{OUT}\right)} \quad (16)$$

In a 15V to 5V converter, for instance, with N = 1/4,

$$\frac{I_{OUT}}{I_{BUCK}} = \frac{15}{5 + 1/4\left(15 - 5\right)} = 2$$

This is a 100% increase in output current.

Maximum switch voltage for a *current-boosted* buck converter is increased from V_{IN} to:

$$V_{SWITCH} = V_{IN} + V_{OUT}/N \quad (17)$$

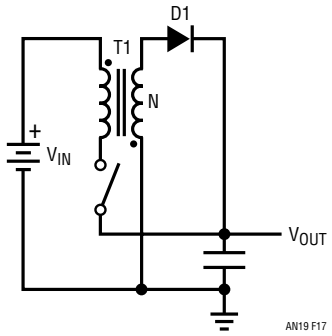


Figure 17. Current-Boosted Buck Converter

APPLICATION CIRCUITS

Boost Mode (Output Voltage Higher Than Input)

The LT1070 will operate in the boost mode with input voltages as low as 3V and output voltages over 50V. Figure 18 shows the basic boost configuration for positive voltages. This circuit is capable of output power levels that depend mainly on input voltage.

$$P_{OUT(MAX)}^{*} \approx V_{IN} \bullet I_P \left[1 - I_P \bullet R\left(\frac{1}{V_{IN}} - \frac{1}{V_{OUT}}\right)\right] \quad (17)$$

* This formula assumes that L1→∞
I_P = maximum switch current
R - switch "on" resistance

With V_{IN} = 5V, V_{OUT} = 12V, I_P = 5A, R = 0.2Ω

$$P_{OUT(MAX)} = 5 \bullet 5\left[1 - 5\left(0.2\right)\left(\frac{1}{5} - \frac{1}{12}\right)\right] = 22W$$

With higher input voltages, output power levels can exceed 100W. Power loss internal to the LT1070 in a boost regulator is approximately equal to:

$$P_{IC} \approx \left(I_{OUT}\right)^2 \bullet R\left[\left(\frac{V_{OUT}}{V_{IN}}\right)^2 - \frac{V_{OUT}}{V_{IN}}\right] + \frac{I_{OUT}\left(V_{OUT} - V_{IN}\right)}{40} \quad (18)$$

The first term of this equation is the power loss due to the "on" resistance of the switch (R). The second term is the loss from the switch driver. For the circuit in Figure 18, with I_{OUT} = 1A:

$$P_{IC} = \left(1\right)^2 \bullet \left(0.2\right)\left[\left(\frac{12}{5}\right)^2 - \frac{12}{5}\right] + \frac{\left(1\right)\left(12 - 5\right)}{40}$$

$$= 0.672 + 0.175 = 0.85W$$

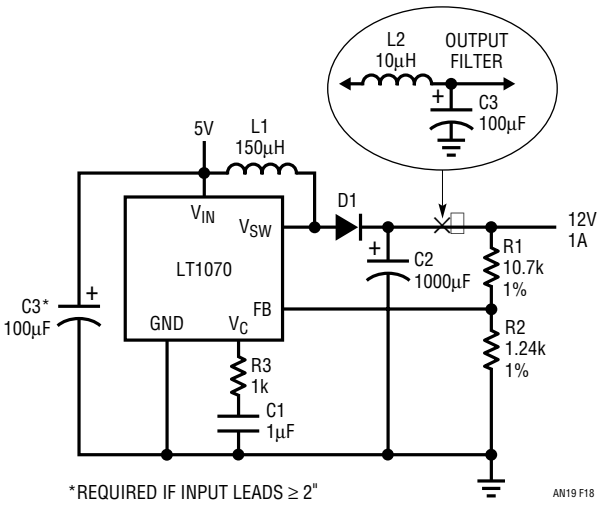


Figure 18. Boost Converter

The only other significant power loss in a boost regulator is in the diode, D1, as given by:

$$P_D = V_F \bullet I_{OUT} \quad (19)$$

V_F is the forward voltage of the diode at a current equal to $I_{OUT} \bullet V_{OUT}/V_{IN}$. In the example shown, with I_{OUT} = 1A and V_F = 0.8V:

$$P_D = 08 \bullet 1 = 0.8W$$

Total power loss in the regulator is the sum of $P_{IC} + P_D$, and this can be used to calculate efficiency (E):

$$E = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{IC} + P_D}$$

$$E = \frac{(1A)(12V)}{(1)(12) + 0.85 + 0.8} = 88\% \quad (20)$$

With higher input voltages, efficiencies can exceed 90%.

Maximum output voltage in the boost mode is limited by the breakdown of the switch to 65V (standard part) or 75V (HV part). It may also be limited by maximum duty cycle if input voltage is low. The 90% maximum duty cycle of the LT1070 limits output voltage to ten times the input voltage. For the simple boost mode, higher ratios of output to input voltage require a tapped inductor.

Design procedure for a boost regulator is straightforward. R1 and R2 set the regulated output voltage. The feedback pin voltage is internally trimmed to 1.244V, so output voltage is equal to 1.244 (R1 + R2)/R2. R2 is normally set to 1.24k and R1 is found from:

$$R1 = R2\left(\frac{V_{OUT}}{1.244} - 1\right) \quad (21)$$

The 1.24k value for R2 is chosen to set divider current at 1mA, but this value can vary from 300Ω to 10k with negligible effect on regulator performance. For proper load regulation, R2 must be returned directly to the ground pin of the LT1070, while R1 is connected directly to the load. For further details, see Pin Description section.

Inductor

Next, L1 is selected. The trade-offs are size, maximum output power, transient response, input filtering, and in some cases, loop stability. Higher inductor values provide maximum output power and low input ripple current, but are physically larger and degrade transient response. Low inductor values have high magnetizing current which reduces maximum output power and increases input current ripple. Low inductance can also cause a subharmonic oscillation problem if duty cycle is above 50%.

With the aforementioned considerations in mind, a simple formula can be derived to calculate L1 based on the maximum ripple current (ΔI) to be allowed in L1.

$$L = \frac{V_{IN}(V_{OUT} - V_{IN})}{\Delta I \bullet f \bullet V_{OUT}} \quad (22)$$

Example: let ΔI = 0.5A, V_{IN} = 5V, V_{OUT} = 12V, f = 40kHz

$$L = \frac{5(5-12)}{(0.5)(40 \bullet 10^3)(12)} = 146\mu H$$

A second formula will allow a calculation of maximum power output with this size inductor:

$$P_{MAX} = V_{IN}\left[I_P - \frac{V_{IN}(V_{OUT} - V_{IN})}{2 \bullet L \bullet f \bullet V_{OUT}}\right]\left[1 - \frac{I_P \bullet R}{V_{IN}} + \frac{I_P \bullet R}{V_{OUT}}\right] \quad (23)$$

I_P = maximum switch current

Using the values from the previous example, with I_P = 5A, R = 0.2Ω,

$$P_{OUT(MAX)} = 5\left[5 - \frac{5(12-5)}{2(146 \bullet 10^{-6})(40 \bullet 10^3)(12)}\right] \times \left[1 - 5 \bullet (0.2)\left(\frac{1}{5} - \frac{1}{12}\right)\right]$$

$$= 5(5 - 0.25)(0.88) = 21W$$

Note that the second term in the first set of brackets is the only one which contains "L," and that this term drops out of the equation for large values of L. In this example, that term is equal to 0.25A, showing that *maximum effective switch current, and therefore maximum output power is reduced by one-half the inductor ripple current in a boost regulator*. In this example, peak effective switch current is reduced from 5A to 4.75A with 0.5A ripple current, a 5% loss. An additional 12% reduction of maximum available power is caused by switch "on" resistance. At higher input voltages, this switch loss is significantly reduced.

When continuous inductor current is desired, the value of L1 cannot be decreased below a certain limit if duty cycle of the switch exceeds 50%. Duty cycle can be calculated from:

$$DC = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (24)$$

In this example,

$$DC = \frac{12-5}{12} = 58.3\%$$

The reason for a lower limit on the value of L for duty cycles greater than 50% is a *subharmonic* oscillation which can occur in current mode switching regulators. For further details of this phenomenon, see Subharmonic Oscillation section of this application section. The minimum value of L1 to ensure no subharmonic oscillations in a boost regulator is:

$$L1_{(MIN)} = \frac{V_{OUT} - 2V_{IN}}{2 \bullet 10^5} = \frac{12-2(5)}{2 \bullet 10^5} = 10\mu H \quad (25)$$

Note that for $V_{OUT} \leq 2V_{IN}$, there is no restriction on inductor size. The minimum value of 10µH obtained in this example is below the value which would yield continuous inductor current, so it is an artificial restriction. Subharmonic oscillations do not occur if inductor current is discontinuous. The critical inductor size for continuous inductor current is:

$$L_{CRIT} = \frac{V_{IN}^2 (V_{OUT} - V_{IN})}{2 \bullet f \bullet I_{OUT} (V_{OUT})^2} = \frac{(5)^2 (12-5)}{2\left(40 \bullet 10^3\right)(1)(12)^2} = 15.2\mu H \quad (26)$$

Discontinuous mode operation is sometimes chosen because it results in the smallest physical size for the inductor. The maximum power output is considerably reduced, however, and can never exceed $2.5(V_{IN})$ watts with the LT1070. The minimum inductor size required to provide a given output power in the discontinuous mode is given by:

$$L_{MIN}(\text{discontinuous}) = \frac{2\, I_{OUT}\left(V_{OUT} - V_{IN}\right)}{I_P^{\,2} \bullet f} \quad (27)$$

Example: let V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 0.5A, I_P = 5A

$$L_{MIN}(\text{discontinuous}) = \frac{\left(2 \bullet 0.5\right)\left(12-5\right)}{\left(5\right)^2 \bullet \left(40 \bullet 10^3\right)} = 7\mu H$$

This formula does not take into account efficiency losses, so the minimum value of L should probably be increased by at least 50% for worst-case conditions. Efficiency is degraded when using minimum inductor sizes because of higher switch and diode peak currents.

In summation, to choose a value for L1:

1. Decide on continuous or discontinuous mode.
2. If continuous mode, calculate C1 based on ripple current and check maximum power and subharmonic limits.
3. If discontinuous mode, calculate L1 based on power output requirements and check to see that output power does not exceed limit for discontinuous mode ($P_{MAX} = 2.5V_{IN}$)

L1 must not saturate at the peak operating current. This value of current can be calculated from:

$$I_{L(PEAK)} = I_{OUT}\frac{\left(V_{OUT}\bullet V_F\right)-\left(I_{OUT}\bullet V_{OUT}\bullet R/V_{IN}\right)}{\left(V_{IN}-I_{OUT}\bullet V_{OUT}\bullet R/V_{IN}\right)} + \frac{V_{IN}\left(V_{OUT}-V_{IN}\right)}{2L1\bullet f\bullet V_{OUT}} \quad (27)$$

V_F = forward voltage of D1
R = "on" resistance of LT1070 switch

In this example, with V_{IN} = 5V, V_{OUT} = 12V, V_F = 0.8V, I_{OUT} = 1A, R = 0.2Ω, L1 = 150µH, f = 40kHz;

$$I_{L(PEAK)} = \frac{1\left(12+0.8-1\bullet 12\bullet (0.2)/5\right)}{5-1\bullet 12\bullet (0.2)/5} + \frac{5\left(12-5\right)}{2\left(150\bullet 10^{-6}\right)\left(40\bullet 10^{3}\right)\left(12\right)}$$

$$= 2.73 + 0.24 = 3A$$

A core must be selected for L1 which does not saturate with 3A peak inductor current.

Output Capacitor

The main criteria for selecting C2 is low ESR (effective series resistance), to minimize output voltage ripple. A reasonable design procedure is to let the *reactance* of the output capacitor contribute no more than 1/3 of the total peak-to-peak output voltage ripple (V_{P-P}), yielding:

$$C2 \geq \frac{V_{OUT}\bullet I_{OUT}}{f\left(V_{IN}+V_{OUT}\right)\left(0.33V_{P-P}\right)} \quad (28)$$

Using V_{OUT} = 12V, I_{OUT} = 1A, V_{IN} = 5V, f = 40kHz and V_{P-P} =200mV,

$$C2 \geq \frac{12\bullet 1}{\left(40\bullet 10^{3}\right)\left(5+12\right)\left(0.33\bullet 0.2\right)} = 268\mu F$$

This leaves 67% of the ripple attributable to ESR, giving:

$$ESR_{(MAX)} = \frac{0.67\bullet V_{P-P}\bullet V_{IN}}{I_{OUT}\left(V_{IN}+V_{OUT}\right)} = \frac{0.67\bullet 0.2\bullet 5}{1\left(5+12\right)} = 0.04\Omega \quad (29)$$

After C2 has been selected, output voltage ripple may be calculated from:

$$V_{P-P} = I_{OUT}\frac{V_{IN}+V_{OUT}}{V_{IN}}\bullet ESR + \frac{V_{OUT}}{\left(V_{IN}+V_{OUT}\right)\left(f\right)\left(C2\right)} \quad (30)$$

If lower output ripple is required, a larger output capacitor must be used with lower ESR. It is often necessary to use capacitor values much higher than calculated to obtain the required ESR. In the example shown, capacitors with guaranteed ESR less than 0.04Ω with a working voltage of 15V generally fall in the 1000µF to 2000µF range. Higher voltage units have lower capacitance for the same ESR.

A second option to reduce output ripple is to add a small LC output filter. If the LC product of the filter is much smaller than L1 • C2, it will not affect loop phase margin. Dramatic reduction in output ripple can be achieved with this filter, often at lower cost and less board space than simply increasing C2. See section on Output Filters for details.

Frequency Compensation

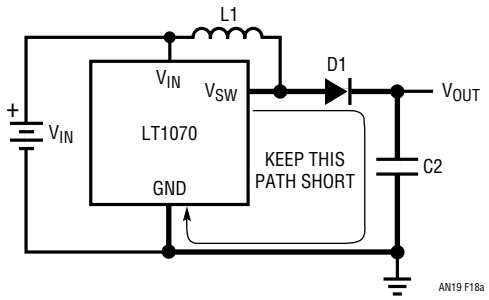
Loop frequency compensation is performed by R3 and C1. Refer to the frequency compensation part of this application section for R3 and C1 selection procedure.

Current Steering Diode

D1 should be a fast turn-off diode. Schottky diodes are best in this regard and offer better efficiency in the forward mode. With higher output voltages, the efficiency aspect is minimal and silicon fast turn-off diodes are a more economical choice. Turn-on time is important also with output voltages above 40V. Diodes with slow turn-on time will have a very high forward voltage for a short time after forward current starts to flow. This transient forward voltage can be anywhere from volts to tens of volts. It must

be summed with output voltage to calculate worst-case switch voltage. To minimize switch transient voltage, the wiring of C2 and D1 should be short and close to the LT1070 as shown below.

Short-Circuit Conditions



Boost regulators are *not* short-circuit protected because the current steering diode (D1) connects the input to the output. The LT1070 will not be harmed for overloads up to 5A. Beyond that point, D1 can be permanently "on" and the LT1070 switch will be effectively shorted to the output. A fuse in series with the input voltage is the only simple means of protecting the circuit. Fuse sizing can be calculated from:

$$I_{IN} \approx \frac{I_{OUT} \bullet V_{OUT}}{V_{IN}} \quad (33)$$

The circuit in Figure 18 has I_{OUT} = 1A, V_{OUT} = 12V, V_{IN} = 5V, yielding:

$$I_{IN} \approx \frac{1 \bullet 12}{5} = 2.4A$$

A 4A fast-blow fuse would be a reasonable choice in this design.

NEGATIVE BUCK CONVERTER

The circuit in Figure 19 is a negative "buck" regulator. It converts a higher negative input voltage to a lower negative output voltage. Buck regulators are characterized by low output voltage ripple, but high input current ripple. The feedback path in this design must include a PNP transistor to level shift the output voltage sense signal to the feedback pin of the LT1070, which is referenced to the negative input voltage.

Output Divider

R1 and R2 set output voltage;

$$R1 = \frac{\left(V_{OUT} - V_{BE}\right)\left(R2\right)}{V_{REF}} \quad (34)$$

V_{REF} = LT1070 reference voltage = 1.244V
V_{BE} = base-emitter voltage of Q1

R2 is nominally set to 1.24k. With the 5.2V output shown,

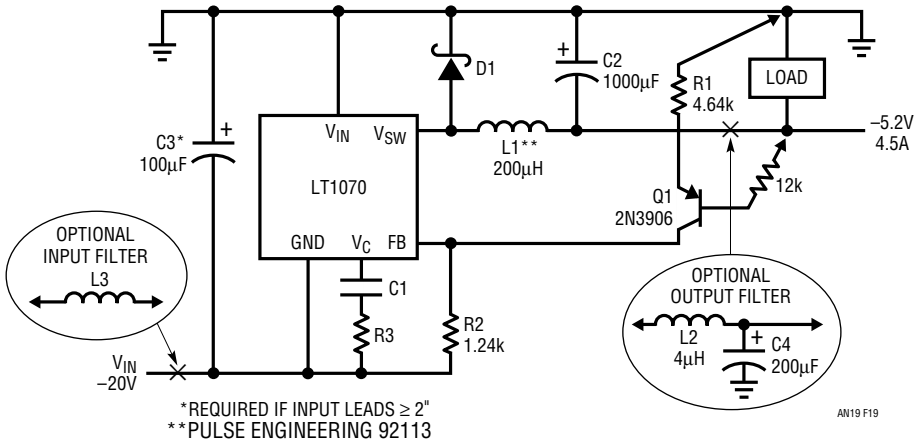


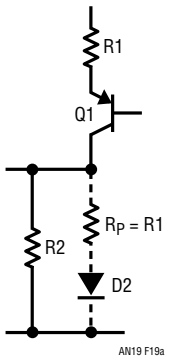
Figure 19. Negative Buck Regulator

and letting V_{BE} = 0.6V, R1 is:

$$R1 = \frac{(5.2 - 0.6)(1.24)}{1.244} = 4.585k\Omega$$

The nearest 1% value is 4.64kΩ. It will be apparent to experienced analog designers that the output voltage will have a temperature drift of 2mV/°C caused by the temperature coefficient of V_{BE}. If this drift is too high, it can be compensated by a resistor/diode network in parallel with R2 as shown.

For zero output drift, R_P is made equal to R1 and R1 is now



calculated from:

$$R1 = R_P = \left(\frac{V_{OUT}}{V_{REF}} - 1\right)(R2) \quad (36)$$

Duty Cycle

Duty cycle of buck converters in the continuous mode is given by:

$$DC = \frac{V_{OUT} + V_F}{V_{IN}}$$

V_F = forward voltage of D1

Inductor

The inductor, L1, is chosen as a trade-off between maximum output power with minimum output voltage ripple, versus small physical size and faster transient response. A good starting point for higher power designs is to choose a ripple current (ΔI). The LT1070 is capable of supplying up to 5A in the buck mode, so a reasonable upper limit on ripple current is 0.5A, or 10% of full load. This sets the value of L1 at:

$$L1 = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{V_{IN}(\Delta I)(f)} \quad (37)$$

With circuit in Figure 19, V_{IN} = 20V, V_{OUT} = 5.2V, f = 40kHz, ΔI = 0.5A, giving:

$$L1 = \frac{(20 - 5.2)(5.2)}{20(0.5)(40 \bullet 10^3)} = 192\mu H$$

The inductor current will go discontinuous (= zero for part of the cycle) when output current is one-half the ripple current. If continuous inductor current is desired for lower load currents, L1 will have to be increased.

Peak inductor and switch current is equal to output current plus one-half the peak-to-peak ripple current;

$$I_{L(PEAK)} = I_{OUT} + \frac{(V_{IN} - V_{OUT})(V_{OUT})}{2(V_{IN})(L)(f)} \quad (37)$$

With the example shown, letting I_{OUT} = 4.5A, L1 = 200μH;

$$I_{L(PEAK)} = 4.5 + \frac{(20 - 5)(5)}{2(20)(200 \bullet 10^{-6})(40 \bullet 10^3)}$$

$$= 4 \bullet 5 + 0.23 = 4.73A$$

The core used for L1 must be sized so that it does not saturate at 4.73A in this example. For lower output current applications, a much smaller core can be used. The core need not be sized for peak current limit conditions (6A to 10A) in most situations because the LT1070 pulse-by-pulse current limit functions even with saturated cores.

Lower values of L1 can be used if maximum output power and low ripple are not as important as physical size or fast transient response. Pure discontinuous mode operation yields the lowest value for L1, and L1 is chosen on the basis of required output current. Maximum output current

in the discontinuous mode is one-half maximum switch current and L1 is found from:

$$L1_{(MIN)} \frac{2V_{OUT}\left(I_{OUT}\right)\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{\left(I_P{}^2\right)(f)} \quad (38)$$

where I_P = maximum switch current.

Example: let V_{OUT} = 5.2V, I_{OUT} = 2A, V_{IN} = 20V, I_P = 5A,

$$L1_{(MIN)} \frac{(2)(5.2)(2)\left(1-\frac{5.2}{20}\right)}{5^2\left(40\bullet10^3\right)} = 15.4\mu H$$

It is suggested that, in discontinuous mode, this calculated value be increased by approximately 50% in practice to account for variations in cores, input voltage and frequency. The core must be sized to not saturate at a peak current of 5A for maximum output in discontinuous mode.

Output Capacitor

C2 is chosen for output ripple considerations. ESR of the capacitor may limit ripple voltage, so this parameter should be checked first. Maximum ESR allowed for a given peak-to-peak output ripple (V_{P-P}), assuming C2 $\rightarrow\infty$, is given by:

$$ESR_{(MAX)} = \frac{V_{P-P}(L1)(f)}{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad (39)$$

with V_{P-P} = 25mV, L1 = 200µH, f = 40kHz, V_{IN} = 20V, V_{OUT} = 5.2V;

$$ESR_{(MAX)} = \frac{0.025\left(200\bullet10^{-6}\right)\left(40\bullet10\right)^3}{5.2\left(1-\frac{5.2}{20}\right)} = 0.052\Omega$$

To obtain a reasonable value for C2, actual ESR should be no more than two-thirds of the maximum value. In this example, ESR is selected at 0.035Ω. C2 may now be found:

$$C2 \geq \frac{1/\left(8Lf^2\right)}{\left[\frac{V_{P-P}}{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}-\frac{ESR}{Lf}\right]} \quad (40)$$

$$\geq \frac{1/\left[8\left(200\bullet10^{-6}\right)\left(40\bullet10^3\right)^2\right]}{\left[\frac{0.025}{5.2\left(1-\frac{5.2}{20}\right)}-\frac{0.025}{\left(200\bullet10^{-6}\right)\left(40\bullet10^3\right)}\right]} \geq 184\mu F$$

It is very likely that a 184µF capacitor of the right operating voltage cannot be found with an ESR of 0.035Ω maximum. C2 will have to be increased in value significantly to achieve the required ESR.

Output Filter

If low output ripple is required, C2 may acquire unreasonably large values. A second option is to add an output filter as shown. Exact calculations for the values of L2 and C4 in this filter are beyond the scope of this note, but a rough approximation can be made by assuming that the ESR of C2 and C4 are the limiting factors. This leads to a value for L2 independent of the actual capacitance of C4.

$$L2 \approx \frac{(ESR2)(ESR4)\left(V_{IN}-V_{OUT}\right)(V_{OUT})}{\left(V_{P-P}\right)(2\pi)(f)^2(L1)(V_{IN})} \quad (41)$$

ESR2 = ESR of C2 and ESR4 = ESR of C4 and V_{P-P} = desired output ripple peak-to-peak.

If we assume ESR2 = ESR4 = 0.1Ω, and require V_{P-P} = 5mV_{P-P};

$$L2 = \frac{(0.1)(0.1)(20-5.2)(5.2)}{(0.005)(2\pi)(40\bullet10^{3})^{2}(200\bullet10^{-6})(20)} = 3.8\mu H$$

L2 may be increased above this value, but the L2 C4 product should be kept at least ten times smaller than L1 C2.

Input Filter

Buck regulators have high ripple current fed back into the input voltage supply. Peak-to-peak value of this current is equal to output current. This can cause intolerable EMI conditions in some systems. An input filter formed by L3 and C3 will greatly reduce this ripple current. The major considerations for this filter are its attenuation ratio and the possible effect it has on the regulator loop stability. See discussion of Input Filters elsewhere in this application section for more details.

Frequency Compensation

R3 and C1 provide frequency compensation. See Frequency Compensation section for details of selecting these components.

Catch Diode

D1 is the current steering diode. During switch off-time, it provides a path for L1 current. This diode should be a high speed switching type with fast turn-on and turn-off. A Schottky type is suggested for lower output voltage applications to improve efficiency. Formulas for average and peak diode current plus diode power dissipation are shown below. These equations assume continuous inductor current with fairly low ripple.

$$I_{PEAK} \approx I_{OUT} \quad (42)$$

$$I_{AV} = I_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (43)$$

$$P_{DIODE} = V_F \bullet I_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (44)$$

where V_F is diode forward voltage at $I = I_{PEAK}$.

NEGATIVE-TO-POSITIVE BUCK-BOOST CONVERTER

The circuit in Figure 20 looks similar to a positive boost regulator except that the output load is referred to the inductor termination (ground) instead of the switch. A transistor (Q1) is used to level shift the output voltage signal down to the feedback pin of the LT1070 which is referred to the negative input voltage.

Unlike buck or boost converters, inverting converters do not have any inherent limitation on input voltage relative to output voltage. Input levels may be either higher or lower than output voltage. The *sum* of input voltage plus output voltage of the LT1070 switch.

Output voltage is given by:

$$V_{OUT} = -V_{IN}\left(\frac{DC}{1-DC}\right) \quad (45)$$

DC = switch duty cycle (0 to 1)

With DC = 0, output voltage is zero, and as DC Æ 1, output voltage increases without limit.

Duty cycle of an inverting buck-boost converter is given by:

$$DC = \frac{|V_{OUT}|}{|V_{IN}| + |V_{OUT}|}$$

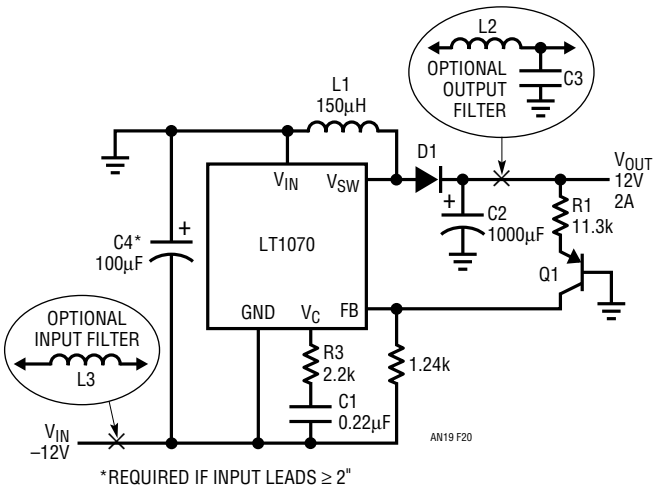


Figure 20. Negative-to-Positive Buck-Boost Converter

Maximum power output of a buck-boost converter is equal to:

$$P_{OUT(MAX)} = \frac{\frac{(I_P)(V_{OUT})(V_{IN})}{V_{OUT}+V_{IN}} - \frac{(I_P)^2(R)(V_{OUT})}{V_{OUT}+V_{IN}}}{1+V_F/V_{OUT}} \quad (46)$$

I_P = peak switch current —1/2 L1 p-p ripple current
R = switch "on" resistance
V_F = forward voltage of D1

The first term on the top of the equation is the theoretical output power with no switch or diode (D1) losses. The second top term is the switch loss. The term on bottom accounts for diode losses.

With the circuit shown, V_{IN} = –12V, V_{OUT} = 12V, ripple current in L1 = $0.5A_{P-P}$, peak switch current = 5A, R = 0.2Ω, V_F = 0.8V,

$$P_{OUT(MAX)} = \frac{\frac{(4.75)(12)(12)}{12+12} - \frac{(4.75)^2(0.2)(12)}{12+12}}{1+0.8/12}$$

$$= 24.6W$$

Setting Output Voltage

R1 and R2 determine output voltage;

$$R1 = \frac{R2(V_{OUT}-V_{BE})}{V_{REF}} \quad (52)$$

V_{REF} = LT1070 reference voltage = 1.244V
V_{BE} = base-emitter voltage of Q1

In this example, R2 = 1.24k, V_{OUT} = 12V, and the V_{BE} of Q1 is ≈ 0.6V, giving:

$$R1 = \frac{1.24(12-0.6)}{1.244} = 11.36k\Omega$$

The output voltage will have a –2mV/°C drift due to the temperature drift of V_{BE}. If this is undesirable, a resistor diode combination can be added in parallel with R2 to correct drift. See section on Negative Buck Converters for details.

Inductor

The inductor is normally calculated on the basis of maximum allowed ripple current, because high ripple currents reduce the maximum available output power and degrade efficiency. For a peak-to-peak ripple current (ΔI_L), L1 is equal to:

$$L1 = \frac{(V_{IN})(V_{OUT})}{(\Delta I_L)(V_{IN}+V_{OUT})(f)} \quad (53)$$

f = LT1070 operating frequency= 40kHz

In this example, with ΔI chosen at 20% of maximum LT1070 switch current (ΔI = 1.0A),

$$L1 = \frac{(12)(12)}{(1.0)(12+12)(40\bullet10^3)} = 150\mu H$$

Larger values for L1 will not raise power levels appreciably, will increase size and cost and will degrade transient response. L1 is not acting as a ripple filter for either the input or the output, so large values will not improve ripple either.

If L1 is reduced in value, maximum power output will be degraded. Equation 46 defines I_P as the maximum allowed switch current minus $1/2\Delta I_L$. Therefore I_P would have to be reduced from 5A to 2.5A if L1 were reduced to the point where the ripple current equaled 5A. This is a 2:1 reduction in maximum output power. Further reductions in L1 result in discontinuous current flow and equation 46 is invalid. The poor efficiency obtained with discontinuous current flow recommends it only for low power outputs when the physical size of L1 is critical. With discontinuous current flow, the minimum recommended size for L1 is:

$$L1_{MIN}(\text{discontinuous}) = \frac{2(V_{OUT})(I_{OUT})}{(f)(0.7I_P)^2} \quad (54)$$

The (0.7) coefficient in form of I_P is a "fudge" factor to account for variations in f and L1, and switching losses.

Example, V_{OUT} = 12V, I_{OUT} = 0.5A, f = 40kHz, I_P = 5A

$$L1 = \frac{2(12)(0.5)}{(40 \bullet 10^3)(0.7 \bullet 5)^2} = 24.5\mu H$$

Once L1 has been selected, peak inductor current in continuous mode can be calculated from:

$$I_{L(PEAK)} = I_{OUT}\left[1 + \frac{V_{OUT} + V_F}{V_{IN} - (I_{OUT} \bullet R)\frac{V_{IN} + V_{OUT}}{V_{IN}}}\right] + \frac{(V_{IN})(V_{OUT})}{2(L1)(V_{IN} + V_{OUT})(f)} \quad (55)$$

V_F = forward voltage of D1
R = LT1070 switch "on" resistance

With the circuit in Figure 20 with L1 = 150µH, V_F = 0.8V, I_{OUT} = 1.5A and R = 0.2Ω,

$$I_{L(PEAK)} = 1.5\left[1 + \frac{12 + 0.8}{12 - (1.5 \bullet 0.2)\frac{12 + 12}{12}}\right] + \frac{(12)(12)}{2(150 \bullet 10^{-6})(12 + 12)(40 \bullet 10^3)}$$

$I_{L(PEAK)}$ = 3.18 + 0.5 = 3.68A

3.18A is the *average* current through L1 and 0.5A is the peak AC ripple current. The core used for L1 must be large enough so that it does not saturate at I_L = 3.68A.

Peak inductor current for discontinuous mode operation is found from:

$$I_{L(PEAK)} = \sqrt{\frac{(I_{OUT})(V_{OUT} + V_F)(2)}{(L1)(f)}} \quad (56)$$

(discontinuous mode)

Example, let L1 = 20µH, I_{OUT} = 0.25A, V_F = 0.8V

$$I_{L(PEAK)} = \sqrt{\frac{(0.25)(12 + 0.8)(2)}{(20 \bullet 10^{-6})(40 \bullet 10^3)}} = 2.83A$$

The core size for this discontinuous application can be considerably smaller than in the previous example. Core volume is approximately proportional to $I_L^2 \bullet L$. With L1 = 100µH, and I_L = 3.93A, $I_L^2 \bullet L = 1.5 \bullet 10^{-3}$. The 20µH inductor with I_L = 2.83A has $I_L^2 \bullet L = 0.16 \bullet 10^{-3}$. The core can be nearly ten times smaller. This size difference is not free—the discontinuous circuit will supply much less current and have somewhat poorer efficiency.

Output Capacitor

C2 must be a high quality (low ESR) switching capacitor because it does all the output filtering. L1 simply functions as an energy transfer element. A reasonable starting point for selecting C2 is to assume that the *ESR* (effective series resistance) of C2 contributes 2/3 of the output ripple and that the *reactance* of C2 contributes 1/3. With this in mind, a formula can be derived for ESR:

$$ESR_{(MAX)} = \frac{(V_{P-P})(V_{IN})(2/3)}{I_{OUT}(V_{IN} + V_{OUT})} \quad (57)$$

V_{P-P} = peak-to-peak output voltage ripple

With V_{P-P} selected at 100mV, and V_{IN} = 12V, V_{OUT} = 12V, I_{OUT} = 1.5A, ESR is:

$$ESR_{(MAX)} = \frac{(0.1)(12)(2/3)}{1.5(12 + 12)} = 0.0185\Omega$$

With ESR found, the value of C2 may now be computed:

$$C2 = \frac{(I_{OUT})(V_{OUT})}{\left[V_{P-P} - (I_{OUT})(ESR)\left(\frac{V_{IN} + V_{OUT}}{V_{IN}}\right)\right](V_{OUT} + V_{IN})(f)} \quad (58)$$

If we specify C2 ESR at 0.015Ω max, C2 is:

$$C2 = \frac{(1.5)(12)}{\left[0.1-(1.5)(0.015)\left(\frac{12+12}{12}\right)\right](12+12)\left(40\bullet 10^3\right)} \quad (59)$$

$$= 341\mu F$$

It is most likely that to find a capacitor with a maximum ESR of 0.015Ω, the capacitance will have to be much larger than 341µF. If lower output ripple is desired, the value of C2 may become very large just to meet ESR requirements.

A second solution to the output ripple problem is to add an output filter at the point indicated in Figure 20. This filter can provide a large reduction in ripple with almost no effect on loop transient response, phase margin or efficiency. See section on Output Filters for further details.

Current Steering Diode

D1 must be a fast recovery diode with an *average* current rating equal to I_{OUT} and peak repetitive rating of I_{OUT} (V_{OUT} + V_{IN})/V_{IN}. If continuous output shorts can occur, D1 must be rated for 10A and heat sunk accordingly unless the LT1070 current limit is externally reduced. Power dissipation of D1 under normal load conditions is:

$$P_{(D1)} = (I_{OUT})(V_F)$$

$$V_F \text{ is D1 forward voltage at } I_D = I_{OUT}\left(\frac{V_{OUT}+V_{IN}}{V_{IN}}\right) \quad (60)$$

Breakdown voltage of D1 must be at least $V_{IN} + V_{OUT}$. Turn-on time should be short to minimize the voltage spike across the LT1070 switch following switch turn-off.

POSITIVE BUCK CONVERTER

Positive buck converters (Figure 21) using the LT1070 require a novel design approach because the negative side of the LT1070 switch is committed to the ground of the chip. This negative switch terminal is the inductor drive point in a positive buck converter. The ground pin of the LT1070 must therefore switch back and forth between the input voltage and converter ground. This is accomplished by tying the positive side of the switch (V_{SW}) to the input supply, and using a peak-detected (C3, D3), bootstrapped supply voltage to operate the chip. As long as the LT1070 is switching, C3 will maintain the chip input-to-ground pin voltage at a voltage equal to the input supply voltage. *It is important to keep the value of C3 to a minimum* to ensure proper start-up of this topology. The 2.2µF value shown should not be increased unless careful tests are done to ensure proper start-up under worst-case *light* loads. If the LT1070 *does not* start, the lightly loaded output will go unregulated high. The minimum recommended load current in any case is 100mA.

The most unusual aspect of this design is the manner in which output voltage information is delivered to the LT1070 feedback pin. This pin is switching along with the LT1070 ground pin to which it is referenced, so the feedback circuit must float on the switching ground pin and at the same

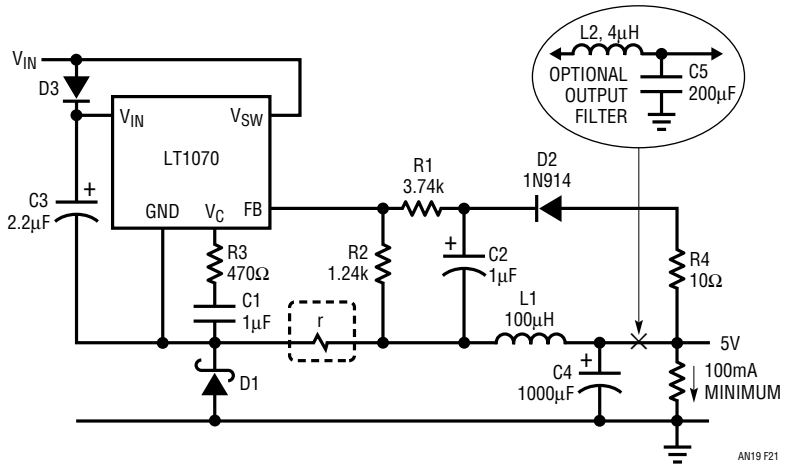


Figure 21. Positive Buck Converter

time be proportional to the DC value of the output voltage. This is accomplished by peak detecting the output voltage with D2 during the "off" time of the LT1070 switch. The voltage on the ground pin of the chip at this time is one diode drop (D1) negative with respect to system ground, because D1 is forward biased by load current flowing through L1. D2 also forward biases, giving a voltage across C2 of:

$$V_{C2} = V_{OUT} - V_{D2} + V_{D1} \quad (61)$$

V_{D1} = forward voltage of D1
V_{D2} = forward voltage of D2

The feedback network, R1/R2, is therefore biased with a voltage very nearly equal to output voltage, and the LT1070 will regulate output voltage according to:

$$V_{OUT} = V_{C2} + V_{D2} - V_{D1} = \frac{V_{REF}(R1+R2)}{R2} + V_{D2} - V_{D1} \quad (62)$$

V_{REF} = reference voltage of LT1070 = 1.244V

If V_{D1} is exactly equal to V_{D2}, output regulation will be perfect, but the forward voltage of D1 is load current dependent, while D2 operates at a fixed average current of 1mA. This can cause output voltage variations of 100mV to 400mV if load current varies over a wide range. To minimize this effect, D1 should be conservatively rated with respect to operating current so that the effect of parasitic series resistance is minimized. The unit shown is rated at 10A average current. D1 should also be a fast turn-on type. (See diode discussion elsewhere in this application section.) A long turn-on time for D1 allows C2 to charge to a voltage *higher* than V_{OUT}, creating an abnormally *low* output voltage. R4 is added to minimize this effect. A Schottky diode is recommended for D1 because these diodes have very fast switching times and their low forward voltage improves efficiency, especially for low output voltage.

Load regulation can be significantly improved in this application by inserting a small resistor (r, shown in dashed box) between D1 and L1. The voltage across r will be equal to (r)(I_{OUT}).This voltage *increases* the voltage across R2, forcing the output voltage to *rise* under load. Perfect load regulation will result if the output *rise* created by r just cancels the output *drop* caused by the increased forward voltage of D1. The required value for r is found from:

$$r = r_d \frac{V_{REF}}{V_{OUT}} \quad (63)$$

r_d = forward series resistance of D1
V_{REF} = LT1070 reference voltage = 1.244V

Load regulation will never be perfect because r_d varies slightly from unit to unit and it is not constant with load current, but regulation better than 2% with V_{OUT} = 5V is easily achieved even with load current varying over a 5:1 range. For higher output voltages, load regulation is even better.

For the circuit shown, with $r_d = 0.05\Omega$, r is:

$$r = \frac{(0.05)(1.244)}{5} = 0.0124\Omega$$

This is most easily obtained by using 9 inches of #22 hookup wire.

Output voltage is determined by R1 and R2:

$$R1 = R2 \frac{V_{OUT} - V_{REF}}{V_{REF}} \quad (64)$$

R2 is normally fixed at 1.24k to set divider current to 1mA. This equation assumes that $V_{D1} = V_{D2}$. A slight adjustment in R1 will be required if $V_{D1} \neq V_{D2}$.

Duty Cycle Limitations

Maximum duty cycle for the LT1070 is 90%. This limits the minimum input voltage in buck regulators. Duty cycle can be calculated from:

$$DC = \frac{V_{OUT} + V_F}{V_{IN} - (I_{OUT} \bullet R) + V_F} \quad (65)$$

V_F = forward voltage of D1
R = "on" resistance of LT1070 switch

Rearranging this formula for V_{IN} yields:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_F}{DC} + (I_{OUT} \bullet R) - V_F \quad (66)$$

With a maximum duty cycle of 90%, (0.9) and V_{OUT} = 5V, V_F = 0.6V, R = 0.2Ω, I_{OUT} = 4A:

$$V_{IN(MIN)} = \frac{5+0.6}{0.9} + \left(0.2 \bullet 4\right) - 0.6 = 6.4V$$

Inductor

The energy storage inductor in a buck regulator functions as both an energy conversion element and as an output ripple filter. This double duty often saves the cost of an additional output filter, but it complicates the process of finding a good compromise for the value of the inductor. Large values give maximum power output and low output ripple voltage, but they also can be bulky and give poor transient response. A reasonable starting point is to select a maximum peak-to-peak ripple current, (ΔI). This yields a value for L1 of:

$$L1 = \frac{\left(V_{IN} - V_{OUT}\right)\left(V_{OUT}\right)}{\left(V_{IN}\right)\left(\Delta I\right)\left(f\right)} \quad (67)$$

f = LT1070 operating frequency ≈ 40kHz

ΔI = peak-to-peak inductor ripple current

With the circuit shown, V_{IN} = 16V, V_{OUT} = 5V and ΔI set at 20% of 3.5A = 0.7A:

$$L1 = \frac{\left(16-5\right)\left(5\right)}{\left(16\right)\left(0.8\right)\left(40 \bullet 10^3\right)} = 122\mu H$$

The ripple current in L1 reduces the maximum output current by one-half ΔI. For lower output currents this is no problem, but for maximum output power, L1 may be raised by a factor of two to three. For lower output powers, L1 can be reduced to save on size and cost. Discontinuous mode operation will occur even near full load if L1 is reduced far enough. The LT1070 is not affected by discontinuous operation per se, but maximum output power is significantly reduced in discontinuous mode designs:

$$I_{OUT(MAX)\ (discontinuous)} = \frac{\left(I_P\right)^2\left(L\right)\left(f\right)}{2V_{OUT}}\left(\frac{V_{IN}}{V_{IN}-V_{OUT}}\right) \quad (68)$$

I_P = LT1070 peak switch current

With L1 = 10µH, for instance, and I_P = 5A:

$$I_{OUT(MAX)} = \frac{\left(5\right)^2\left(10 \bullet 10^{-6}\right)\left(40 \bullet 10^3\right)}{2\left(5\right)}\left(\frac{16}{16-5}\right) = 1.4A$$

Efficiency is also reduced with discontinuous operation because of increased switch dissipation.

The load current where a buck regulator changes from continuous to discontinuous operation is:

$$I_{CRIT} = \frac{\left(V_{IN} - V_{OUT}\right)\left(V_{OUT}\right)}{2\left(V_{IN}\right)\left(f\right)\left(L1\right)} \quad (69)$$

With a 100µH value of L1, inductor current will go discontinuous at:

$$I_{CRIT} = \frac{\left(16-5\right)\left(5\right)}{2\left(16\right)\left(40 \bullet 10^3\right)\left(100 \bullet 10^{-6}\right)} = 0.43A \quad (70)$$

I_{CRIT} can never exceed 2.5A (one half maximum LT1070 switch current).

Peak inductor current in a buck regulator with continuous mode operation is:

$$I_{L(PEAK)} = I_{OUT} + \frac{\left(V_{IN} - V_{OUT}\right)\left(V_{OUT}\right)}{2\left(V_{IN}\right)\left(L1\right)\left(f\right)} \quad (71)$$

With I_{OUT} = 3.5A and L1 = 100µH:

$$I_{L(PEAK)} = 3.5 + \frac{\left(16-5\right)\left(5\right)}{2\left(16\right)\left(100 \bullet 10^{-6}\right)\left(40 \bullet 10^3\right)} = 3.93A$$

The core used for L1 must be able to handle 3.93A peak current without saturating.

Peak inductor currents in discontinuous mode are much higher than output current:

$$I_{L(PEAK)\ (discontinuous)} = \sqrt{\frac{2\left(V_{OUT}\right)\left(I_{OUT}\right)\left(V_{IN}-V_{OUT}\right)}{\left(V_{IN}\right)\left(L1\right)\left(f\right)}} \quad (72)$$

For L1 = 10µH, I_{OUT} = 1A:

$$I_{L(PEAK)} = \text{(discontinuous)} \sqrt{\frac{2(5)(1)(16-5)}{(16)(10 \bullet 10^{-6})(40 \bullet 10^{3})}} = 4.15A$$

The 10µH inductor, at 1A output current, must be sized to handle 4.14A peak current.

Output Voltage Ripple

See Negative Buck Regulator section for calculation of output ripple.

Output Capacitor

C4 is chosen for output voltage ripple considerations. Its ESR (effective series resistance) is the most important parameter. For details, see Negative Buck Regulators section.

Output Filter

For very low output voltage ripple, the value of C4 may become prohibitively high. An output filter, L2 and C5, may be used to reduce output ripple. See Output Filter section for details.

FLYBACK CONVERTER

Flyback converters (Figure 22) are able to regulate an output voltage either higher or lower than the input voltage by shuttling stored energy back and forth between the windings of a transformer. During switch "on" time, all energy is stored in the primary winding according to: $E = (I_{PRI})^2(L_{PRI})/2$. When the switch turns off, this energy is transferred to the output winding. The current in the secondary just after switch opening is equal to the reciprocal of turns ratio (1/N) times the current in the primary just prior to switch opening. Output voltage of a flyback converter is not constrained by input voltage as in buck or boost converters.

$$V_{OUT} = \frac{DC}{1-DC}\left(N \bullet V_{IN}\right) \quad (73)$$

$$DC = \text{switch duty cycle} = \frac{V_{OUT}}{V_{OUT} + \left(N \bullet V_{IN}\right)} \quad (74)$$

N = transformer turns ratio

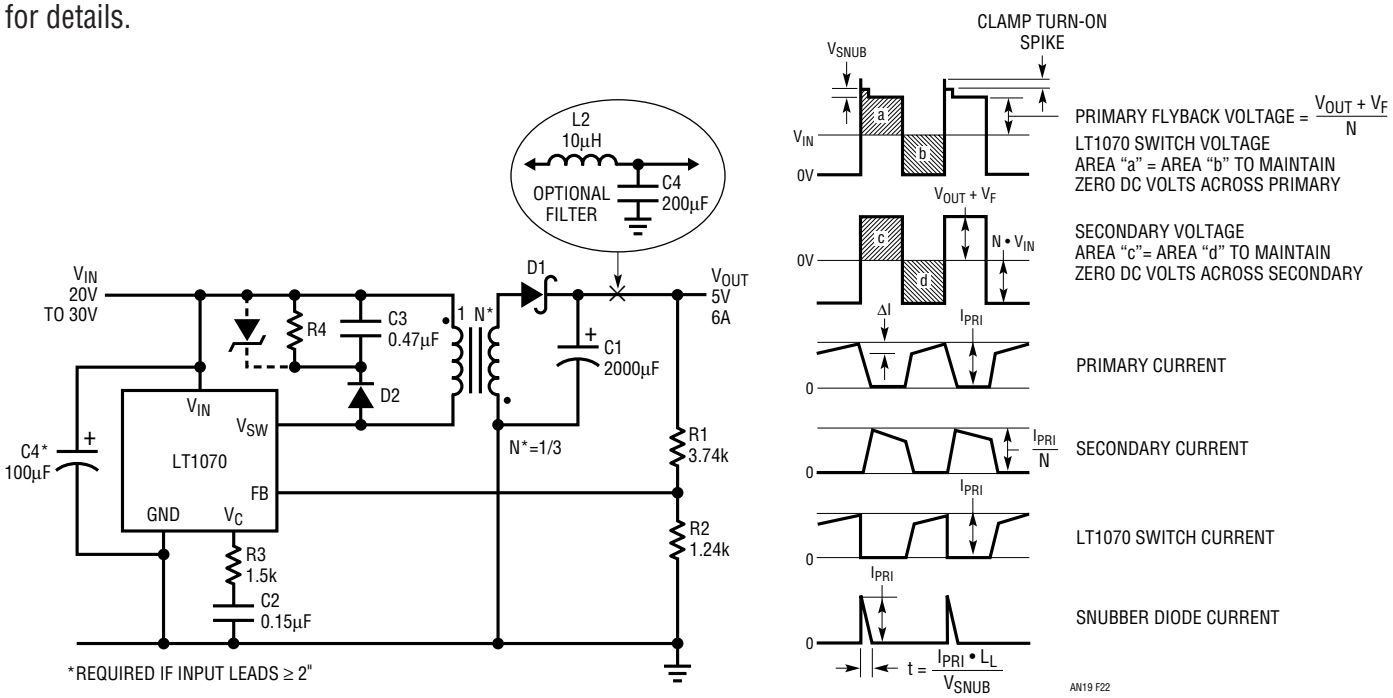


Figure 22. Flyback Converter

By varying duty cycle between 0 and 1, output voltage can theoretically be set anywhere from 0 to ∞. Practically, however, output voltage is constrained by switch breakdown voltage and the maximum output voltage is limited to:

$$V_{OUT(MAX)} = N\left(V_M - V_{SNUB} - V_{IN}\right) \quad (75)$$

V_{SNUB} = snubber voltage (see snubber details in this section)
V_M = maximum allowed switch voltage

This still allows the LT1070 to regulate output voltages of hundreds or even thousands of volts by using large values of N.

In many applications, N can vary over a wide range without degrading performance. If maximum output power is desired however, N can be optimized:

$$N_{(OPT)} = \frac{V_{OUT} + V_F}{V_M - V_{IN(MAX)} - V_{SNUB}} \quad (76)$$

V_F = forward voltage of D1

In Figure 22, with V_{OUT} = 5V, V_F = 0.7V (Schottky), $V_{IN(MAX)}$ = 30V, V_M = 60V, V_{SNUB} = 15V;

$$N_{(OPT)} = \frac{5 + 0.7}{60 - 30 - 15} = 0.38$$

A turns ratio of 1:3 (0.33) was used in this circuit.

A second important transformer parameter which must be determined is primary inductance (L_{PRI}). For maximum output power, L_{PRI} should be high to minimize magnetizing current, but this can lead to unacceptably large core sizes. A reasonable design approach is to reduce the value of L_{PRI} to the point where primary magnetizing current (ΔI) is about 20% of peak switch current. The LT1070 is rated for 5A peak switch current, so for full power applications, ΔI can be set to 1A peak-to-peak. Maximum output current is reduced by one-half of the ratio of ΔI to peak switch current, or ≈10% in this case.

With this design approach, L_{PRI} is found from:

$$L_{PRI} = \frac{(V_{IN})(V_{OUT})}{(\Delta I)(f)(V_{OUT} + N \bullet V_{IN})} \quad (77)$$

With V_{IN} = 24V, V_{OUT} = 5V, ΔI = 1A, N = 1/3:

$$L_{PRI} = \frac{(24)(5)}{(1)\left(40 \bullet 10^3\right)(5 + 1/3 \bullet 24)} = 231\mu H$$

Values of L_{PRI} higher than this will raise maximum output current only slightly and will require larger core size. Lower primary inductance may be used for lower output currents to reduce core size.

Maximum output current is a function of peak allowed switch current (I_P):

$$I_{OUT(MAX)} = \frac{E\left(I_P - \frac{\Delta I}{2}\right)(V_{IN})}{(N \bullet V_{IN}) + V_{OUT}} \quad (78)$$

I_P = maximum LT1070 switch current
E = overall efficiency ≈ 75%

With V_{IN} = 24V, V_{OUT} = 5V, I_P = 5A, ΔI = 1A, N = 1/3:

$$I_{OUT(MAX)} = \frac{0.75\left(5 - \frac{1}{2}\right)(24)}{(1/3 \bullet 24) + 5} = 6.2A$$

The 75% efficiency number comes from losses in the snubber network (≈6%), LT1070 switch (≈4%), LT1070 driver (≈3%), output diode (≈8%) and transformer (≈4%). Although this efficiency is not as impressive as the 85% to 95% obtainable with simple buck or boost designs, it is more than justified in many cases by the ability to use the variable N to generate high output currents or high output voltages and the option to add extra windings for multiple outputs.

Peak primary current is used to determine core sizing for the transformer:

$$I_{PRI} = \frac{I_{OUT}}{E}\left(\frac{V_{OUT}}{V_{IN}} + N\right) + \frac{(V_{IN})(V_{OUT})}{2(f)(L_{PRI})(V_{OUT} + N \bullet V_{IN})} \quad (79)$$

For an output current of 6A, with V_{IN} = 24V, V_{OUT} = 5V, E = 75%, L_{PRI} = 231µH, N = 1/3:

$$I_{PRI} = \frac{6}{0.75}\left(\frac{5}{24} + 1/3\right) + \frac{(24)(6)}{2\left(40 \bullet 10^3\right)\left(231 \bullet 10^{-6}\right)\left(5 + 1/3 \bullet 24\right)}$$

$$= 4.33 + 0.5 = 4.83A$$

The core must be able to handle 4.83A peak current in the 231µH primary winding without saturating. (See section on inductors and transformers for further details.)

Output Divider

R1 and R2 set output voltage:

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \bullet R2 \quad (80)$$

V_{REF} = feedback reference voltage of the LT1070 = 1.244V

R1 and R2 can vary over a wide range, but a convenient value for R2 is 1.24k, a standard 1% value.

For a 5V output,

$$R1 = \frac{(5 - 1.244)(1.24)}{1.244} = 3.756k\Omega$$

Frequency Compensation

R3 and C2 provide a pole-zero frequency compensation. For details, see the section on frequency compensation elsewhere in this application note.

Snubber Design

Flyback converters using transformers require a clamp to protect the switch from overvoltage spikes. These spikes are created by leakage inductance in the transformer. Leakage inductance (L_L) is modeled as an inductor in series with the primary winding which is not coupled to the secondary as shown in Figure 23.

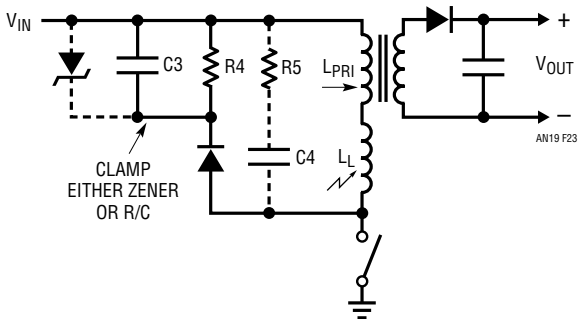


Figure 23. Snubber Clamping

During switch "on" time, a current is established in L_L equal to peak primary current (I_{PRI}). When the switch turns off, the energy stored in L_L, ($E = I^2 \bullet L_L/2$) will cause the switch voltage to fly up to breakdown if the voltage is not clamped.

If a Zener diode is used for clamping, Zener clamp voltage is selected by assigning a maximum switch voltage and maximum input voltage:

$V_{ZENER} = V_M - V_{IN(MAX)}$

V_M = maximum allowed switch voltage

The standard LT1070 maximum switch voltage is 65V, so V_M is typically set at 60V to allow a margin of 5V. If we assume $V_{IN(MAX)}$ = 30V for this circuit:

V_{ZENER} = 60 – 30 = 30V

Peak Zener current is equal to peak primary current (I_{PRI}) and average power dissipation is equal to:

$$P_{ZENER} = \frac{(V_Z)(I_{PRI})^2(L_L)(f)}{2\left(V_Z - \frac{V_{OUT} + V_F}{N}\right)} \quad (81)$$

An important part of this equation is the term [$V_Z - (V_{OUT} + V_F)/N$] in the denominator. This voltage is defined as snubber voltage (V_{SNUB}) and is the difference between the Zener voltage and the normal flyback voltage of the primary. (See waveforms with Figure 22.) If V_{SNUB} is too low, Zener dissipation rises rapidly. A reasonable minimum for V_{SNUB} is 10V, so this should be checked before proceeding further:

$$V_{SNUB} = V_Z - \frac{V_{OUT} + V_F}{N} = 30 - \frac{5 + 0.7}{1/3} = 12.9V \quad (82)$$

Leakage inductance in a transformer can be minimized by bifilar winding or by interleaving the primary and secondary. If this is done correctly, leakage inductance is usually less than 1% of primary inductance. If we wind T1 for L_{PRI} = 230µH, L_L should be less than 2.3µH. Using this value, power dissipation in the Zener at full load current is:

$$P_{ZENER} = \frac{(30)(4.83)^2(2.3 \bullet 10^{-6})(40 \bullet 10^3)}{2\left(30 - \frac{5 + 0.7}{1/3}\right)} = 2.5W$$

Zener dissipation under short-circuit conditions is calculated from the same equation (81) by assuming that V_{OUT} = 0V and I_{PRI} is the current limit value of the LT1070. If we let I_{PRI} = 9A:

$$P_{ZENER} \text{ (output shorted)} = \frac{(30)(9)^2(3.5 \bullet 10^{-6})(40 \bullet 10^3)}{2\left(30 - \frac{0.7}{1/3}\right)} = 4W$$

The waveform of LT1070 switch voltage shows a narrow spike extending above the snubber clamp voltage. This spike is caused by the turn-on time of the clamp circuit, in particular the diode in series with the Zener. This diode should be a Schottky or a very fast turn-on type to minimize the height of this spike. It must be rated for peak currents equal to I_{PRI}. The reverse voltage rating of the diode must be at least $V_{IN(MAX)}$.

An alternative to Zener clamping is an R/C clamp. This is less expensive, but has the disadvantage of a less well-defined clamping level. The RC snubber also dissipates power even with no-load conditions. A value for R4 is found from:

$$R_{SNUB} = \frac{2(V_R)^2 - 2(V_R)(V_{OUT}/N)}{(I_{PRI})^2(L_L)(f)} \quad (83)$$

V_R = voltage across snubber resistor

If we set V_R = 30V (same as V_{ZENER}) and use full load conditions of I_{PRI} = 4.83A:

$$R_{SNUB} = \frac{2(30)^2 - 2(30)\left(\frac{5}{1/3}\right)}{(4.83)^2(2.3 \bullet 10^{-6})(40 \bullet 10^3)} = 419\Omega$$

Power dissipation in the snubber at full load is equal to:

$$P_R = \frac{(V_R)^2}{R} = \frac{(30)^2}{419} = 2.15W$$

At very light loads, the voltage across the snubber resistor drops to the flyback voltage of the primary, $V_R = (V_{OUT} + V_F)/N$.

In this example, flyback voltage is 16.8V, resulting in a snubber dissipation of $16.8^2/419\Omega$ = 0.67W.

This may be a consideration where high efficiency is necessary even with near-zero output loads. *Short circuit* power dissipation in the snubber resistor is approximately equal to:

$$P_R \approx \frac{(I_{PRI})^2(f)(L_L)}{2} \quad (84)$$

(output shorted)

I_{PRI} in short circuit is the current limit of the LT1070. For I_{PRI} = 9A, snubber dissipation with the output shorted is ≈3.7W in this example.

The value of C3 is not critical, but it should be large enough to keep the ripple voltage across the snubber to only a few volts. This yields a capacitor value of:

$$C3 = \frac{V_R}{(R)(f)(V_S)} \quad (85)$$

V_S = voltage ripple across C3

For V_S = 3V, V_R = 30V, R = 419Ω:

$$C3 = \frac{30}{(419)(40 \bullet 10^3)(3)} = 0.6\mu F$$

C3 should be a very low ESR (effective series resistance)

film or ceramic type to keep spike voltage to a minimum.

C4 and R5 (shown in dashed lines) form an optional damper, which eliminates primary ringing for light output load conditions when secondary current drops to zero during switch-off time (discontinuous operation). Typical values are R = 300Ω to 1.5k, C = 500pF to 5000pF.

Output Diode (D1)

The output diode has an *average* forward current equal to output current, but the current flows in pulses with an amplitude equal to:

$$I_{D1(PEAK)} = I_{OUT}\left(1+\frac{V_{OUT}+V_F}{N\left(V_{IN}\right)}\right) \quad (86)$$

For the circuit in Figure 22, with I_{OUT} = 6A:

$$I_{D1(PEAK)} = 6\left(1+\frac{5+0.7}{1/3\left(24\right)}\right) = 10.3A$$

To calculate diode power dissipation, use the forward voltage at this peak current multiplied times output current;

$P_{D1}=(V_F)(I_{OUT})$

V_F = D1 forward voltage at peak current

With V_F = 0.55V and I_{OUT} = 6A, D1 power dissipation is 3.3W.

During start-up and overload conditions, D1 current will increase significantly. *Average* diode current through D1 when the LT1070 is in current limit is equal to:

$$I_{D1} = \frac{\alpha\left(I_{LIM}\right)\left(V_{IN}\right)}{N\left(V_{IN}\right)+V_{OUT}+V_F} \quad (87)$$

(during LT1070 current limit)

α is an empirical multiplier slightly less than unity. It is very complex to calculate, but it takes into account such things as switch resistance, leakage inductance, snubber losses, and transformer losses. If we assume α = 0.8, I_{LIM} = 9A, V_{IN} = 24V, N = 1/3, V_F = 0.55V and a shorted output (V_{OUT} = 0V):

$$I_{D1} = \frac{0.8\left(9\right)\left(24\right)}{1/3\left(24\right)+0+0.8} = 20A$$

Peak diode current will be only slightly higher because the duty cycle of the diode is approaching 100% with V_{OUT} = 0V.

Output short-circuit current can be reduced, if desired, by clamping the V_C pin of the LT1070. The best way to do this and still be assured of maximum full-load current is to clamp the V_C pin to a portion of output voltage. This generates a foldback current limit that will reduce short-circuit current without affecting normal load current. The clamp network in Figure 24 will reduce shorted output current of the circuit in Figure 22 to ≈5A.

The clamp point is generated by splitting R1 into two resistors such that the tap point voltage is ≈1.75V at normal output voltage. This ensures that D4 will not turn on until the output voltage begins to drop. When V_{OUT} = 0V, the voltage at the FB pin is clamped to approximately 0.35V by the internal mode select circuitry and the voltage at the R1 tap point will be approximately the same. The current through the diodes will be maximum available V_C pin current. This sets the clamp voltage on the V_C pin at ≈1.55V, reducing output short-circuit current to ≈5A. Full-load current can be reduced, if desired, by moving the tap point on R1 down, even to the point where it becomes part of R2.

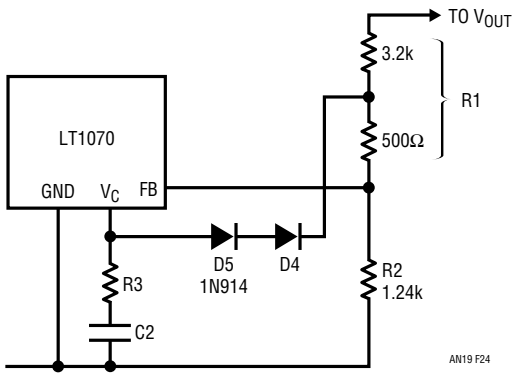


Figure 24. Foldback Current Limiting

Output Capacitor (C1)

Flyback converters do not use the inductance of the transformer as a filter, so the output capacitor must do all the filtering work. The output peak-to-peak voltage ripple is equal to:

$$V_{P-P} = \frac{I_{OUT}}{(f)(C1)\left(1+\frac{N(V_{IN})}{V_{OUT}}\right)} + (ESR)(I_{OUT})\left(1+\frac{V_{OUT}}{N(V_{IN})}\right) \quad (88)$$

ESR = effective series resistance of C1

The first term is the ripple due to the *capacitance* of C1; the second term is ripple due solely to the ESR of the capacitor. As it turns out, commercially available capacitors in the range required for this application (100µF to 10,000µF) have ESR high enough to dominate the ripple voltage. A 2,000µF capacitor for instance, might have a guaranteed ESR of 0.02Ω. For I_{OUT} = 6A, V_{OUT} = 5V, V_{IN} = 24V, N = 1/3, this gives:

$$V_{P-P} = \frac{6}{\left(40\bullet10^{3}\right)\left(2000\bullet10^{-6}\right)\left(1+\frac{1/3(24)}{5}\right)} + (0.02)(6)\left(1+\frac{5}{1/3(24)}\right)$$

$$= 28.8mV + 195mV = 224mV$$

The ESR term dominates and will be the main criteria for selecting the size of the output capacitor.

An alternative to brute force output capacitance (to obtain low ESR) is to add an LC output filter (shown as L1 and C4 in Figure 22). A relatively small inductor and capacitor can greatly reduce output ripple. If we assume the ripple across C1 is due solely to ESR, and therefore rectangular, the ratio of filter output ripple to input ripple is:

$$\frac{V_{OUT(P-P)}}{V_{IN(P-P)}} = r = \frac{ESR4(V_{OUT})(N\bullet V_{IN})}{(L1)(f)(V_{OUT}+N\bullet V_{IN})^{2}} \quad (89)$$

ESR4 = effective series resistance of C4

This formula again assumes that the ESR of C4 dominates its total impedance. For ESR4 = 0.1Ω, L1 = 10µH, V_{OUT} = 5V, N = 1/3, V_{IN} = 24V,

$$r = \frac{(0.1)(5)(1/3\bullet24)}{\left(10\bullet10^{-6}\right)\left(40\bullet10^{3}\right)(5+1/3\bullet24)^{2}} = 0.059$$

This is a 16:1 reduction in ripple, greatly easing the requirements on C1. Total output ripple, with a filter, is given by:

$$V_{P-P} = \frac{(ESR1)(ESR4)(V_{OUT})(I_{OUT})}{(L1)(f)(V_{OUT}+N\bullet V_{IN})} \quad (90)$$

For ESR1 = 0.05Ω, ESR4 = 0.1Ω, V_{OUT} = 5V, V_{IN} = 24V, N = 1/3, I_{OUT} = 6A, L1 = 10µH, output ripple (P-P) is:

$$V_{P-P} = \frac{(0.05)(0.01)(5)(6)}{\left(10\bullet10^{-6}\right)\left(40\bullet10^{3}\right)(5+1/3\bullet24)} = 28.8mV$$

TOTALLY ISOLATED CONVERTER

The LT1070 has a second operating mode called "isolated flyback," as shown in Figure 25 (see Note 1 with figure). While in this mode, it does not use the feedback pin to sense output voltage; instead, it senses and regulates the transformer primary voltage during switch "off" time (t_{OFF}). This voltage is related to V_{OUT} by:

$$V_{OUT} = (N)(V_{PRI}) - V_F$$

(during t_{OFF}) (90)

N = turns ratio of transformer
V_F = forward voltage of output diode
V_{PRI} = primary voltage during switch "off" time

The secondary output voltage will be regulated if V_{PRI} is regulated. The LT1070 switches from normal mode to regulated primary mode when the current *out* of the feedback pin exceeds ≈10µA. An internal clamp holds the voltage (V_{FB}) on this pin at ≈400mV. R2 is used to put the LT1070 in isolated flyback mode. It also doubles as an adjustment in the regulated output. V_{PRI} is regulated to 16V + 7k (V_{FB}/R2), where V_{FB}/R2 is equal to the current

through R2, and the 7k is an internal resistor. V_{OUT} is therefore equal to:

$$V_{OUT} = N\left[16 + 7k\left(\frac{V_{FB}}{R2}\right)\right] - V_F \quad (91)$$

and the required transformer turns ratio is:

$$N = \frac{V_{OUT} + V_F}{16 + 7k\left(\frac{V_{FB}}{R2}\right)} \quad (92)$$

The term, 7k (V_{FB}/R2) is normally set to ≈2V to allow some adjustment range in V_{OUT}. Solving for N in Figure 25, with V_{OUT} = 15V:

$$N = \frac{15 + 0.7}{16 + 2} = 0.872$$

The smallest integer ratio with N close to 0.872 is 7:8 = 0.875. T1 is to be wound with this turns *ratio* for each output. The *total* number of turns is determined by the required primary inductance (L_{PRI}). This inductance has no optimum value; it is a trade-off between core size, regulation requirements and leakage inductance effects. A reasonable starting value is found by assigning a maximum magnetizing current (ΔI) of 10% of the peak switch current of the LT1070. Magnetizing current is the difference between the primary current at the start of switch "on" time and the current at the end of switch "on" time. This gives a value for L_{PRI} of:

$$L_{PRI} = \frac{V_{IN}}{(\Delta I)(f)\left(1 + \frac{V_{IN}}{V_{PRI}}\right)} \quad (93)$$

ΔI = primary magnetizing current
V_{PRI} = regulated primary flyback voltage

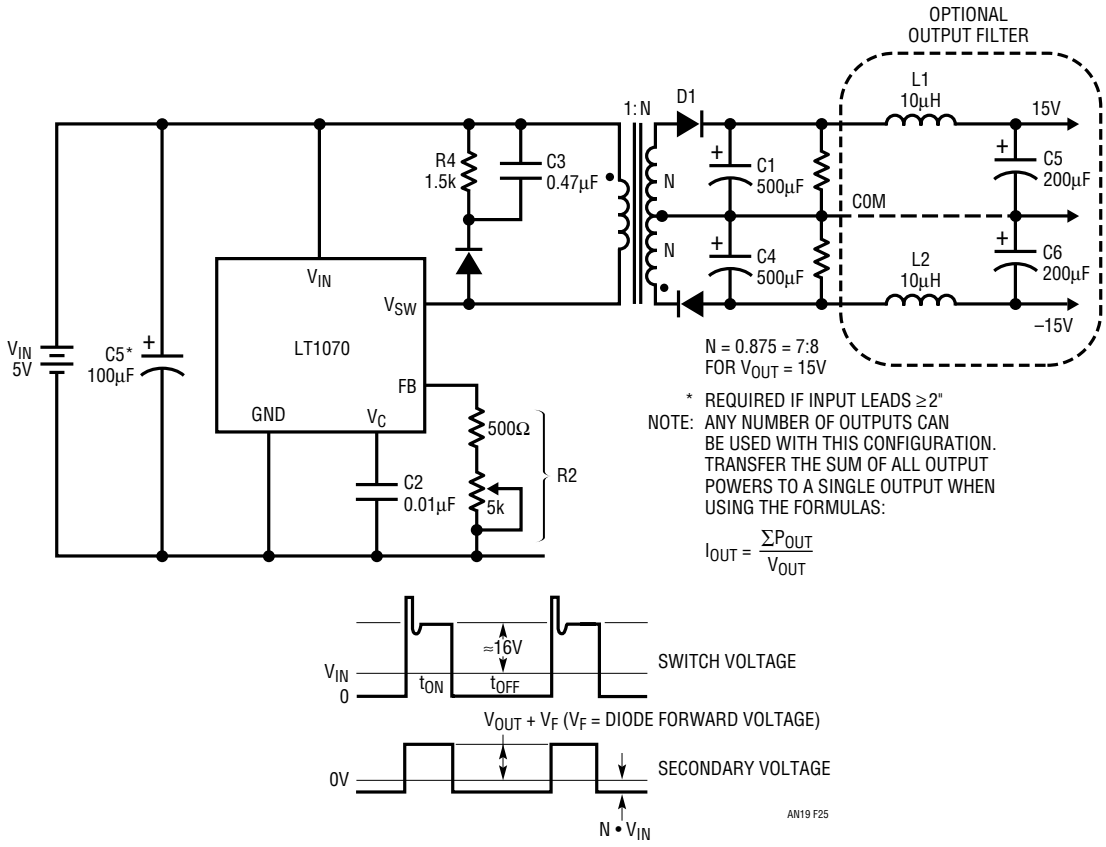


Figure 25. Totally Isolated Converter

For V_{IN} = 5V, ΔI = 0.5A, V_{PRI} = 18V:

$$L_{PRI} = \frac{5}{(0.5)\left(40 \bullet 10^3\right)(1+5/18)} = 196\mu H$$

Again, this value is not an optimum figure, it is simply a compromise between maximum output current and core size.

A second consideration on primary inductance is the transition from continuous mode to discontinuous mode. At light output loads, the flyback pulse across the primary will drop toward zero before the end of switch "off" time. The LT1070 interprets this as a drop in output voltage and raises duty cycle to compensate. This results in an abnormally high output voltage. To avoid this situation, the output should have a minimum load equal to:

$$I_{OUT(MIN)} = \frac{\left(V_{PRI} \bullet V_{IN}\right)^2}{\left(V_{PRI} + V_{IN}\right)^2 (2V_{OUT})(f)(L_{PRI})} \quad (94)$$

with V_{PRI} = 18V, V_{IN} = 5V, V_{OUT} = 15V, L_{PRI} = 200µH:

$$I_{OUT(MIN)} = \frac{\left(18 \bullet 5\right)^2}{\left(18+5\right)^2 (2 \bullet 15)\left(40 \bullet 10^3\right)\left(200 \bullet 10^{-6}\right)}$$

$$= 64mA$$

This current may be shared equally on each output at 32mA per output. If a lighter minimum load is desired, primary inductance must be increased. This also increases leakage inductance, so some care must be used.

Leakage inductance is a portion of the primary which is not coupled to the secondary. This leakage inductance will create a flyback spike following switch opening. The height of this spike must be clamped with a snubber (R4, C3, D2) to avoid overvoltage on the switch. (Please read snubber details in the section on normal mode flyback regulators). The *width* of the leakage inductance spike is equal to:

$$t_L = \frac{(I_{PRI})(L_L)}{V_M - V_{PRI} - V_{IN}} \quad (95)$$

L_L = leakage inductance
I_{PRI} = peak primary current
V_M = peak switch voltage

This spike width is important because it must be less than 1.5µs wide. The LT1070 has internal blanking for ≈1.5µs following switch turn-off. This blanking time ensures that the flyback error amplifier will not interpret the leakage inductance spike as the actual flyback voltage to be regulated. To avoid poor regulation, the spike must be less than the blanking time.

If transformer T1 is trifilar wound for minimum leakage inductance, L_L may have a typical value of 1.5% of L_{PRI}. Assuming L_{PRI} = 200µH, L_L would be 3µH. To calculate t_L, we still need to assign a value to V_M. In this case, with V_{IN} = 5V, a conservative value for maximum switch voltage would be V_M = 50V. If we assume a maximum primary current of 5A for maximum output current, spike width is:

$$t_L = \frac{5\left(3 \bullet 10^{-6}\right)}{50 - 18 - 5} = 0.56\mu s$$

This is well within the maximum value of 1.5µs. Note, however, that the pulse width grows rapidly as the sum of V_{PRI} + V_{IN} approaches maximum switch voltage. The following formula will allow one to calculate the maximum ratio of leakage inductance to primary inductance in a given situation.

$$\frac{L_L}{L_P}(MAX) = \frac{t_L\left(V_M - V_P - V_{IN}\right)(\Delta I)(f)\left(1 + \frac{V_{IN}}{V_P}\right)}{I_{PRI}\left(V_{IN}\right)} \quad (96)$$

With a fairly large V_{IN} (36V), even if we use a less conservative value of 60V for V_M, with t_L = 1.5µs, V_P = 18V, ΔI = 0.5A and I_{PRI} = 5A:

$$\frac{L_L}{L_P}(MAX) = \frac{\left(1.5 \bullet 10^{-6}\right)(60 - 18 - 36)(0.5)\left(40 \bullet 10^3\right)\left(1 + \frac{36}{18}\right)}{5(36)}$$

$$= 0.003 = 0.3\%$$

This low ratio of leakage inductance to primary inductance would be nearly impossible to wind, so some compromises must be made. If maximum output current is not required, I_{PRI} will be less than 5A, (see formula 99). Ripple current (ΔI) can also be increased. Finally, an LT1070HV (high voltage) part can be used, with a switch rating of 75V. Substituting I_{PRI} = 2.5A, ΔI = 1A, V_M = 70V into the above calculation yields L_L/L_{PRI} = 3%, which is easily achievable.

Maximum output power with an isolated flyback converter is less than an ordinary flyback converter because transformer turns ratio is fixed by output voltage. This fixes duty cycle at:

$$DC = \frac{V_{PRI}}{V_{PRI} + V_{IN}} \quad (97)$$

and maximum power is limited to:

$$P_{OUT(MAX)} = \left(\frac{V_{PRI}}{V_{PRI} + V_{IN}}\right)\left[V_{IN}\left(I_P - \frac{\Delta I}{2}\right) - \left(I_P\right)^2 R\right]\left(0.8\right) \quad (98)$$

R = LT1070 Switch "on" resistance
I_P = maximum switch current
0.8 = fudge factor to account for losses in addition to R

With V_{PRI} at a nominal 18V, V_{IN} = 5V, I_P = 5A, ΔI = 0.5A, duty cycle is 78% and maximum output power is:

$$P_{OUT(MAX)} = \left(\frac{18}{18+5}\right)\left[5\left(5 - \frac{0.5}{2}\right) - \left(5\right)^2\left(0.2\right)\right]\left(0.8\right) = 11.74W$$

An analysis of the power formula shows that at low V_{IN}, maximum output power is proportional to V_{IN}, and at high V_{IN}, maximum power approaches 50W.

Peak primary current for loads less than the maximum is found from:

$$I_{PRI} = \frac{\left(V_{OUT}\right)\left(I_{OUT}\right)\left(V_{PRI} + V_{IN}\right)}{0.8\left(V_{PRI}\right)\left(V_{IN}\right)} + \frac{\Delta I}{2} + \boxed{\frac{\left(I_{PRI}\right)^2 R}{V_{IN}}} \quad (99)$$

This formula is actually a quadratic, but rather than solve it explicitly, a much simpler technique, for the range of I_{PRI} involved, is to calculate the first two terms on the right, then use this value of I_{PRI} to calculate the last term. For the circuit in Figure 25 with I_{OUT} = 0.25A on each output, V_{PRI} = 18V, V_{IN} = 5V, ΔI = 0.5A, R = 0.2Ω:

$$I_{PRI} = \underbrace{\frac{\left(15\right)\left(0.5\right)\left(18+5\right)}{0.8\left(18\right)\left(5\right)}}_{2.64A} + \frac{0.5}{2} + \frac{\left(2.64\right)^2\left(0.2\right)}{5} = 2.92A$$

The transformer must be sized so that the core does not saturate with 2.92A in the primary winding. Note that there is plenty of margin on 5A maximum switch current. A smaller core could be used if ΔI were increased to 1A, cutting primary inductance in half. (See section on inductors and transformers.)

Output Capacitors

Flyback regulators do not utilize the inductance of the transformer as a filter, so all filtering must be done by the output capacitors, C1 and C4. They should be low ESR types to minimize output ripple. In general, output ripple is limited by the ESR of the capacitor, not the actual capacitance. Output ripple in peak-to-peak volts is given by:

$$V_{P-P} = \frac{I_{PRI}}{2 * N}\left(ESR\right) \quad (100)$$

*This factor of 2 is used because of dual outputs

With I_{PRI} = 2.92A, N = 0.872 and assigning an ESR of 0.1Ω, output ripple is:

$$V_{P-P} = \frac{\left(2.92\right)\left(0.1\right)}{\left(2\right)\left(0.872\right)} = 167mV_{P-P} \text{ at full load}$$

Had we based the output ripple formula on the actual output *capacitance*, rather than its ESR, the result would have been ≈10mV, showing that ESR effects do dominate. The 0.1Ω value chosen for ESR is probably *higher than*

typical for a good 500µF capacitor, but *less than guaranteed maximum*. Note that one reason for high output ripple in this circuit is that the converter is operating at a rather high duty cycle of 78% because of the low input voltage. This leaves only 22% of the time for the secondary to be delivering current to the load. As a consequence, secondary peak currents, and therefore output ripple, are high.

If low output ripple is required, an output filter may be a better choice than simply using huge output capacitors. See Output Filters section.

Load and Line Regulation

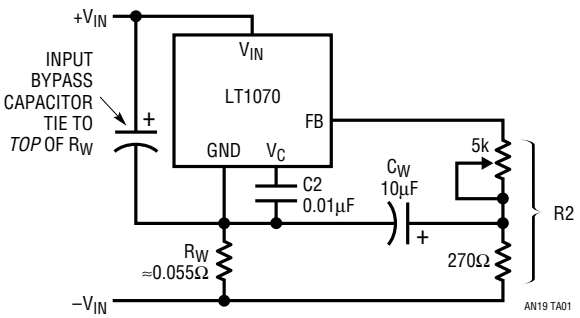
Load and line regulation are affected by many "open loop" factors in this circuit because the actual output voltage is not sensed—only the primary. Some of these factors are core nonlinearities, diode resistance, leakage inductance, winding resistance, (including skin effect) capacitor ESR and secondary inductance. A typical load regulation for this circuit with a load variation from 20% to 100% is ≈3%. Line regulation at light loads is better than 0.3% for V_{IN} = 4.5V to 5.5V, but degrades to ≈1% for full loads.

With multiple output supplies obtained from a single switching loop, the problem of cross regulation appears. In this supply, and *increase* in load current from 50mA to 200mA on one output, with a constant 50mA load on the second output, will cause the loaded output to *drop* 280mV and the constant load output to *rise* 100mV.

If improved line and load regulation are necessary, a modification can be made to the basic circuit as shown below:

R2 is split into two resistors with the center tap coupled to the ground pin of the LT1070 through C_W. A small resistor

Load Current Compensation



R_W is inserted in series with the ground pin. When a load is applied to the output, input current flowing through R_W causes the voltage drop across R2 to increase. This increases regulated primary voltage and thereby output voltage, cancelling the open-loop load regulation effects mentioned earlier. Line regulation is also significantly improved at full load.

The value of R_W is found from:

$$R_W = \frac{(R_O)(V_{IN})(E)(R2)}{(V_{OUT})(7k)(N)^*} \quad (101)$$

R_O = output resistance without compensation
= $\Delta V_{OUT}/\Delta I_{OUT}$

E = efficiency ≈0.75

*Multiply N by two for dual outputs

For the circuit in Figure 25, R_O is found by loading both outputs simultaneously and summing the changes of the two outputs. With 3% load regulation, at ΔI_{OUT} = 200mA, this is a total output change of 900mV. R_O is then 900mV divided by a current change of 200mA, or 4.5Ω. V_{OUT} is the sum of the two outputs, =30V, N is (0.875)(2) = 1.75 and R2 is ≈1.2k:

$$R_W = \frac{(4.5)(5)(0.75)(1{,}200)}{(30)(7k)(1.75)} = 0.055\Omega$$

This low value of resistance preserves the efficiency of the converter, but is sometimes hard to find "off the shelf." A 15" length of #26 hookup wire was used for the breadboard. To minimize inductance, the wire is folded in half before winding around a form.

C_W must be made large enough to prevent loop oscillation problems. The product of C_W times the parallel resistance of the two halves of R2 should be several times larger than the basic regulator settling time constant.

With load regulation compensation, the effects of cross regulation are worse than with no compensation. Multiple output supplies should be carefully evaluated for all expected conditions of output loading.

Frequency Compensation

The frequency compensation capacitor C2, is much lower in this design than in others because the g_m of the LT1070 is much lower in the isolated mode than in the normal mode. See Frequency Compensation section for details.

POSITIVE CURRENT-BOOSTED BUCK CONVERTER

A current-boosted buck converter is shown in Figure 26. It can supply more output current than a standard buck converter or a flyback converter for larger input-output differentials because current flows to the output both when the switch is on *and* when it is off. The "on" cycle can supply up to 5A to the load. The off cycle will deliver 1/N times that much current. With N = 1/3, current delivered to the load during switch off time will be 15A. Total available load current will depend on switch duty cycle, which in turn is fixed by input voltage.

An operational amplifier must be added to generate a feedback signal which floats on top of the regulated output because that is where the ground pin of the LT1070 is tied. A1 is an LM308 selected because its output goes *low* when both its inputs are equal to the op amp negative supply voltage. This condition occurs at V_{OUT} = 0V during start-up. If the op amp output went *high* during this condition, the LT1070 would never start up. R1 and R2 set output voltage, with the bottom of R1 returned directly to the load for "low" sensing. R4 and R5 force Kelvin sensing between the output and the ground pin of the LT1070. It appears that these resistors are shorted out, but the voltage drop across the wire from the ground pin of the LT1070 to the output will cause load regulation problems unless it is "sensed" by R4 and R5. These resistors can be eliminated if that wire is heavy gauge and less than 2" long.

The following equations should be helpful in designing variations of this circuit.

$$R5 = \frac{(V_{OUT})(R1)}{V_{REF}} = \frac{(V_{OUT})(1.24k)}{1.244V} \quad (102)$$

$$\frac{R5}{R4} = \frac{R1}{R2} \quad (103)$$

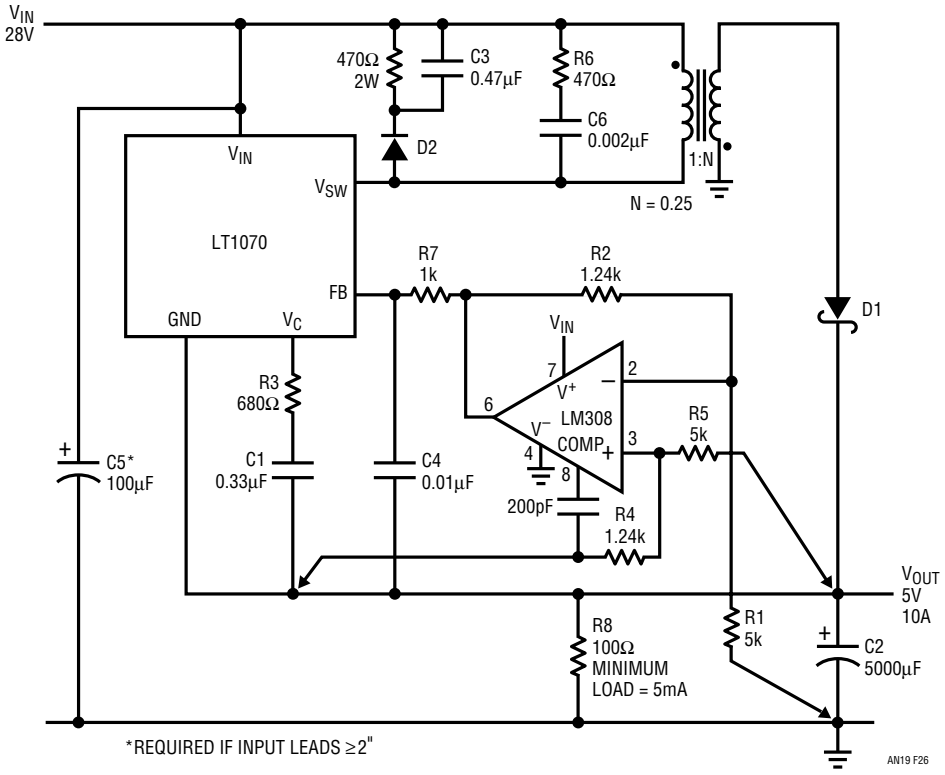


Figure 26. Positive Current Boosted Buck Converter

$$N_{(MIN)} = \frac{V_{OUT} + V_F}{V_M - V_{IN} - V_{SNUB}} \quad (104)$$

$$DC = \frac{V_{OUT} + V_F}{V_{OUT} + V_F + N\left(V_{IN} - V_{OUT}\right)} \quad (105)$$

$$L_{PRI} = \frac{V_{OUT}}{\left(\Delta I\right)\left(f\right)\left(N + \frac{V_{OUT}}{V_{IN} - V_{OUT}}\right)} \quad (106)$$

$$V_{P-P} = \left(ESR\right)\left(I_{OUT}\right)\frac{\left(\frac{V_{OUT}}{N} + V_{IN} - V_{OUT}\right)\left(1-N\right)}{V_{IN}} \quad (107)$$

$$I_{OUT(MAX)} = \left(I_P - \frac{\Delta I}{2}\right)\left[\frac{V_{IN}}{V_{OUT} + V_F + N\left(V_{IN} - V_{OUT}\right)}\right]\left(0.8\right) \quad (108)$$

$$I_{PRI} = \frac{I_{OUT}}{V_{IN}}\left[V_{OUT} + N\left(V_{IN} - V_{OUT}\right)\right] \quad (109)$$

(Add ΔI/2 for peak primary current)

N = turns ratio
V_M = LT1070 maximum switch voltage
V_{SNUB} = snubber voltage (see Flyback section)
V_F = forward voltage of D1
DC = switch duty cycle
ΔI = peak-to-peak primary ripple current
ESR = effective series resistance of C2
I_{PRI} = average primary current during switch-on time
V_{P-P} = peak-to-peak output ripple voltage
I_P = maximum rated switch current for LT1070

The value for N_{MIN} is based on switch breakdown. Low values give higher output current, but also higher switch voltage. ΔI is normally chosen at 20% to 40% of I_{PRI}. Note that the ripple equation contains the term (1 – N) in the numerator, implying that output ripple current and voltage will be zero for N = 1. This is because of the simplifying assumption that ripple current into the output capacitor is the *difference* between primary and secondary current. This difference is zero for N = 1 and the equation is no longer valid.

NEGATIVE CURRENT-BOOSTED BUCK CONVERTER

The negative buck converter in Figure 27 is capable of much higher output current that the standard buck converter upper limit of 5A. For design details, see Positive Current-Boosted Buck Converter and standard Negative Buck Converter sections.

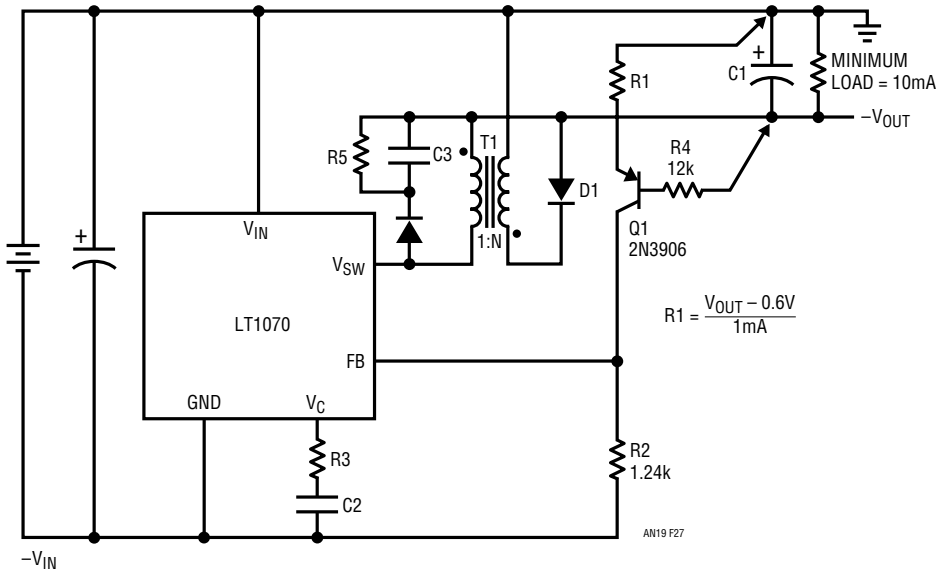


Figure 27. Negative Current Boosted Buck Converter

NEGATIVE INPUT/NEGATIVE OUTPUT FLYBACK CONVERTER

This circuit in Figure 28 is normally used for negative output voltages *higher* than the negative input. If voltages *lower* than the input are required, see Negative Buck Converter or Negative Current-Boosted Buck Converter and standard Negative Buck Converter sections.

The voltage divider, R1 and R2, is required to prevent forward bias on Q1. Connect R1, R2 and R3 exactly as shown for proper output sensing. Further design details may be taken from Positive Flyback Converter section.

POSITIVE-TO-NEGATIVE FLYBACK CONVERTER

The positive input-negative output flyback converter in Figure 29 requires an external op amp to generate the feedback signal for the LT1070. R1 and R2 set output voltage with R1 scaled at 1kΩ/V. The bottom of R1 goes directly to the output for sensing. R3 and R4 provide the

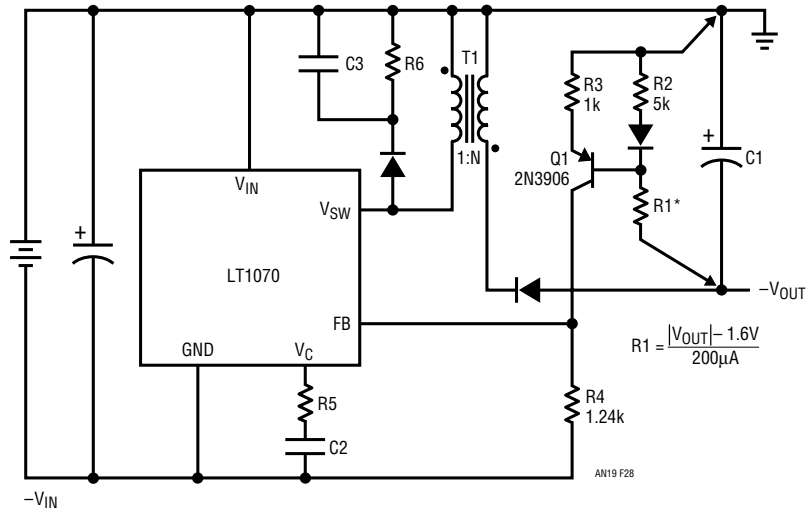


Figure 28. Negative Input-Negative Output Flyback Converter

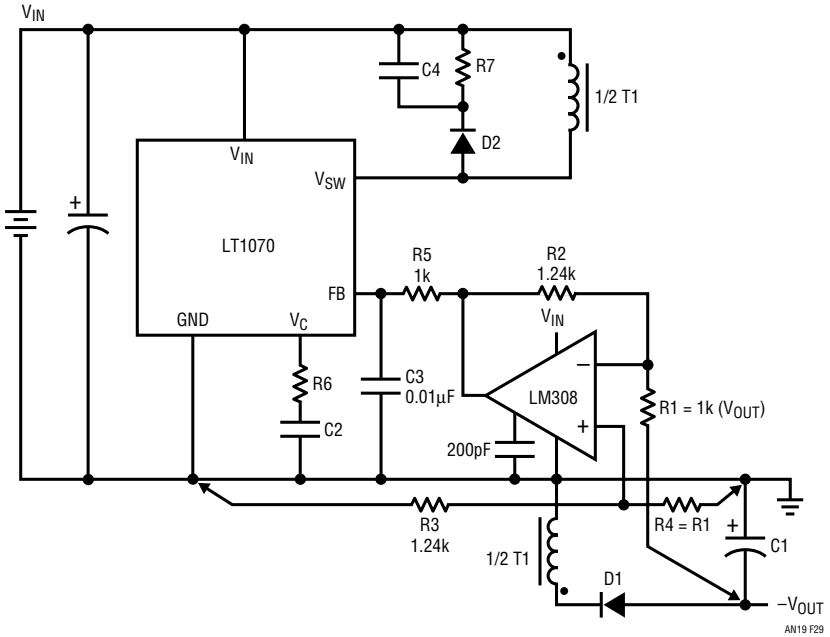


Figure 29. Positive Input-Negative Output Flyback Converter

ground (low) sense. Any voltage drop between the ground pin of the LT1070 and the actual ground (+) output can cause load regulation problems. These are eliminated if R3 and R4 are connected exactly as shown. R3 and R4 can be eliminated if the LT1070 ground pin is connected directly to output ground with a very short heavy wire. For design details, see Positive Flyback Converter.

VOLTAGE-BOOSTED BOOST CONVERTER

The standard boost converter has a maximum output voltage slightly less than the maximum switch voltage of the LT1070. If higher voltages are desired, the inductor can be tapped as shown in Figure 30. The effect of the tap is to reduce peak switch voltage by:

$$\left(V_{OUT} - V_{IN}\right)\left(\frac{N}{1+N}\right) \text{ volts}$$

A large value for N will allow high output voltages to be regulated without exceeding maximum switch voltage.

A snubber is needed now to handle leakage inductance of the tap point. The following formulas will be helpful for variations on this design.

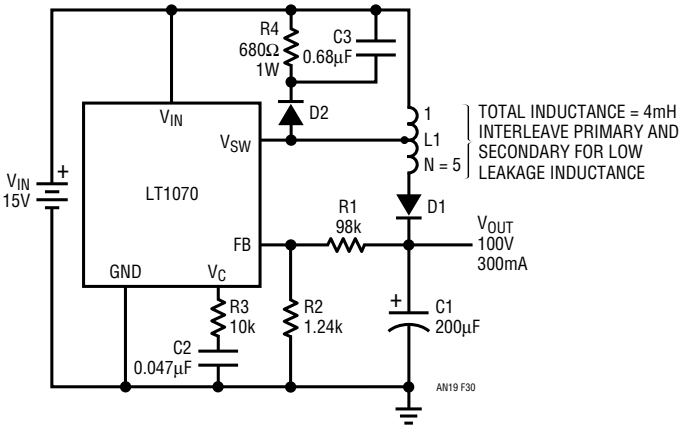


Figure 30. Voltage-Boosted Boost Converter

$$N_{(MIN)} = \frac{V_{OUT} - V_M + V_{SNUB}}{V_M - V_{IN} - V_{SNUB}} \quad (\text{use max } V_{IN}) \tag{110}$$

$$DC = \frac{V_{OUT} - V_{IN}}{V_{OUT} + N\left(V_{IN}\right)} \tag{111}$$

$$I_{OUT(MAX)} = \frac{I_P \frac{\Delta I}{2}\left(V_{IN}\right)}{V_{OUT} + N\left(V_{IN}\right)} \tag{112}$$

$$I_{PRI} = \frac{I_{OUT}\left[V_{OUT} + N\left(V_{IN}\right)\right]}{V_{IN}} \tag{113}$$

Average during switch-on time. For peak, add ΔI/2.

$$L_{PRI} = \frac{V_{IN}\left(V_{OUT} - V_{IN}\right)}{\left(\Delta I\right)\left(f\right)\left[V_{OUT} + N\left(V_{IN}\right)\right]} \tag{114}$$

$\Delta I \approx 20\%$ to 40% of I_{PRI}

$$V_{P\text{-}P} = \frac{\left(I_{OUT}\right)\left(ESR\right)\left[V_{OUT} + N\left(V_{IN}\right)\right]}{V_{IN}\left(N+1\right)} \tag{115}$$

DC = switch duty cycle
V_{SNUB} = snubber voltage (see Flyback section for details)
V_M = maximum allowed LT1070 switch voltage
I_P = maximum LT1070 switch current
ΔI = peak-to-peak primary current ripple
ESR = effective series resistance of C
$V_{P\text{-}P}$ = peak-to-peak output voltage ripple

L1 should be wound for minimum leakage inductance by using bifilar winding or interleaved windings. R3 and C2 are selected using the technique described in the frequency compensation section. For snubber details see Flyback description section. This regulator is not short-circuit proof because L1 and D1 short input to ground when output is shorted.

NEGATIVE BOOST CONVERTER

The LT1070 can be used as a negative boost regulator as shown in Figure 31 by using the same diode-coupled feedback technique used in the positive buck mode. Basically, D2 and C3 create a peak detector which gives a voltage across C3 equal to the output voltage. R1 and R2 act as a voltage divider to set output voltage at:

$(V_{REF})(R1 + R2)/R2$

C3 also acts as a floating power supply for the LT1070. The ground pin of the LT1070 switches back and forth between the output voltage and ground to drive the inductor, L1. For proper circuit operation, a minimum preload of 10mA is required on the output (shown as R_O).

For further design information, see Positive Boost Converter section for details on L1, C1, D1 and output filters. The feedback scheme used here is discussed in more detail in the Positive Buck section. A refinement in the feedback is that the power transistor driver current flowing into the V_{IN} pin must come from D2 and C3. This tends to compensate for the series resistance of D1 as it affects load regulation.

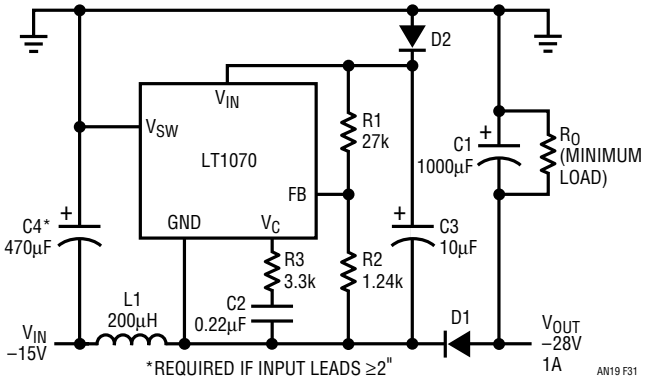


Figure 31. Negative Boost Regulator

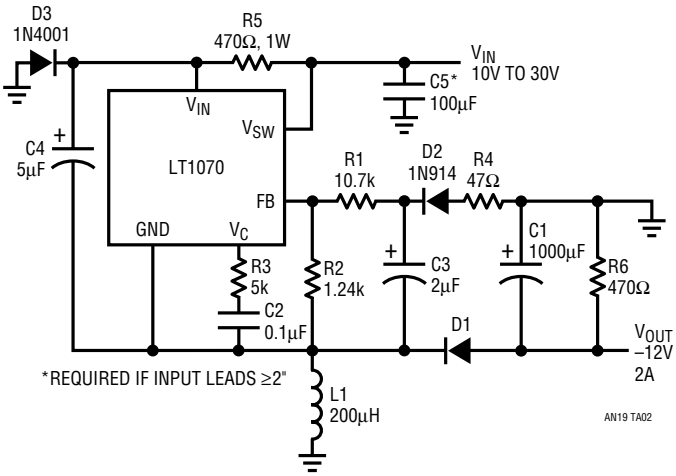
POSITIVE-TO-NEGATIVE BUCK BOOST CONVERTER

This positive-to-negative converter uses the same feedback technique as the positive buck converter. Normal feedback cannot be used because the ground pin of LT1070 is switching back and forth between $+V_{IN}$ and $-V_{OUT}$. To generate a floating feedback signal, D2 peak detects the output voltage during the LT1070 switch-off time. This voltage appears across C3 as a floating DC level which is used as feedback to the LT1070. Output voltage is set by the ratio of R1 to R2. R4 is used to limit the effect of turn-on spikes across the main catch diode, D1. Without this resistor, D1 turn-on spikes would cause C3 to charge to an abnormally high voltage and the output voltage would sag down at high load currents.

D3 and C4 are used to generate a floating supply for the LT1070. The voltage across C4 will peak detect to (V_{OUT}) volts. R5 is added to ensure start-up. R6 is a preload, required only if the normal load can drop to zero current.

For further design details on this circuit, the basic formulas from the Negative-to-Positive Buck/Boost Converter may be used, along with the feedback explanation from the Positive Buck Converter.

Positive-to-Negative Buck Boost Converter



CURRENT-BOOSTED BOOST CONVERTER

This tapped inductor version of the boost converter can offer significant increases in output power when the input-output voltage differential is not too high. The ratio of output current for this converter compared to a standard boost converter is:

$$\frac{I_{OUT}}{I_{BOOST}} = \frac{N+1}{N\left(1-\frac{V_{IN}}{V_{OUT}}\right)+1}$$

If $V_{OUT} \rightarrow V_{IN}$, the increase in output current approaches N + 1. Maximum N, however, is limited by switch breakdown voltage;

$$N_{(MAX)} = \frac{V_M - V_{OUT} - V_{SNUB}}{V_{OUT} - V_{MIN}}$$

V_M = maximum LT1070 switch voltage
V_{SNUB} = snubber voltage (see Flyback section)
V_{MIN} = minimum input voltage

For V_M = 60V, V_{OUT} = 28V, V_{SNUB} = 8V, V_{MIN} = 16V,

$$N_{(MAX)} = \frac{60 - 28 - 8}{28 - 16} = 2$$

The increase in output current is:

$$\frac{I_{OUT}}{I_{BOOST}} = \frac{2+1}{2\left(1 - \frac{16}{28}\right)+1} = 1.62 = 62\%$$

Actual maximum output current is:

$$I_{OUT(MAX)} = \frac{I_P - \Delta I/2}{\frac{V_{OUT}}{V_{MIN}} - \frac{N}{N+1}} = \frac{5 - 0.5}{\frac{28}{16} - \frac{2}{3}} = 4.15A$$

I_P = maximum LT1070 switch current
ΔI = increase in inductor current during switch-on time

$$\Delta I = \frac{V_{OUT} - V_{IN}}{(L)(f)\left(\frac{V_{OUT}}{V_{IN}} - \frac{N}{N+1}\right)}$$

L = total inductance

Operating duty cycle is given by:

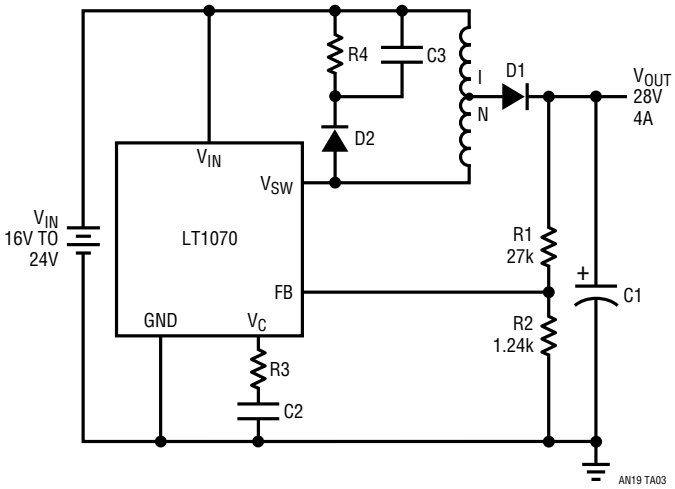
$$DC = \frac{V_{OUT} - V_{IN}}{V_{OUT} - \left(\frac{N}{N+1}\right)(V_{IN})}$$

A reasonable value for total inductance is found by assuming that this circuit is used near peak switch current of 5A and allowing a 20% increase in switch current during switch on time→ΔI = 1A:

$$L_{TOTAL} = \frac{V_{OUT} - V_{MIN}}{(f)(\Delta I)\left(\frac{V_{OUT}}{V_{MIN}} - \frac{N}{N+1}\right)} = \frac{28 - 16}{\left(40 \bullet 10^3\right)(1)\left(\frac{28}{16} - \frac{2}{3}\right)} = 277\mu H$$

Snubber values are empirically selected to limit snubber voltage to the value chosen (≈8V). For lowest snubber losses, the "1" and "N" sections of the inductor should be wound for maximum coupling (consult manufacturers).

Current-Boosted Boost Converter



FORWARD CONVERTER

Forward converters can use smaller cores than flyback converters because they do not need to store energy in the core. Energy is transferred directly to the output during switch "on" time. The output secondary (N) is positive and delivering current through D1 when the LT1070 switch is on (V_{SW} low). At switch turn-off, the output winding goes negative and output current flows through D2 as in a buck regulator. A third winding (M) is needed in a single switch forward converter to define switch voltage during switch-off time. This "reset" winding, however, limits the maximum duty cycle allowed for the switch. The voltage across the switch during its off state is:

$$V_{SW} = V_{IN} + \frac{V_{IN}}{M} + V_{SNUB}$$

V_{SNUB} = snubber voltage spike caused by leakage inductance

By rearranging this formula, a minimum value for M can be found:

$$M_{(MIN)} = \frac{V_{IN(MAX)}}{V_M - V_{IN(MAX)} - V_{SNUB}}$$

V_M = maximum LT1070 switch voltage
$V_{IN(MAX)}$ = maximum input voltage

For the circuit shown, with $V_{IN(MAX)}$ = 30V, and selecting V_{SNUB} = 5V and V_M = 60V:

$$M_{(MIN)} = \frac{30}{60 - 30 - 5} = 1.2$$

The value of M will define maximum switch duty cycle. If the LT1070 attempts to operate at a duty cycle above this limit, the core will saturate because the volt-second product across the primary in the switch-off state will not be enough to keep flux balance. Duty cycle is limited to:

$$DC_{(MAX)} \frac{1}{1+M} = \frac{1}{1+1.2} = 45\%$$

For maximum output current, N should be as small as possible. Smaller values of N, however, require larger duty cycles, so N is limited to a minimum of:

$$N_{(MIN)} = \frac{(M+1)(V_{OUT} + V_F)}{V_{IN(LOW)}}$$

V_F = D1 and D2 forward voltage
$V_{IN(LOW)}$ = minimum input voltage

For the circuit shown, with V_F = 0.6V, $V_{IN(LOW)}$ = 20V:

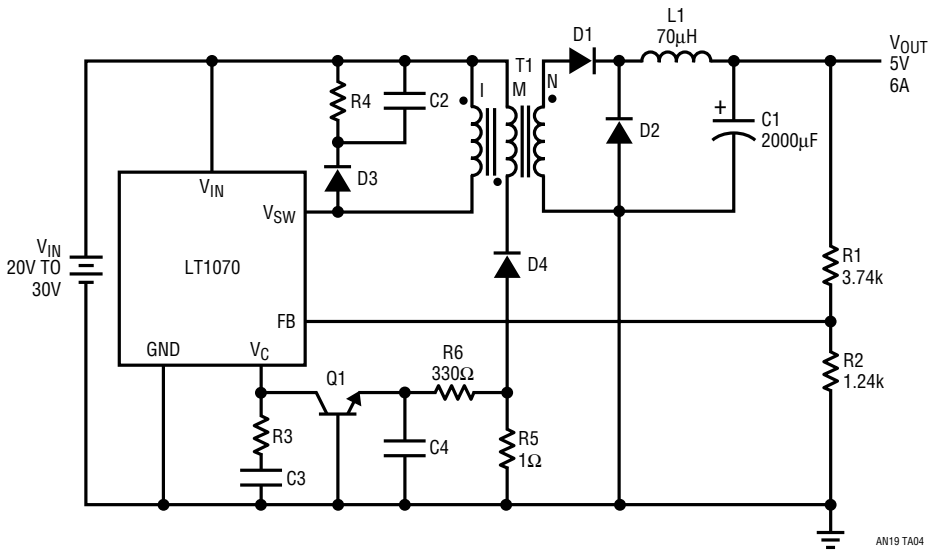
$$N_{(MIN)} = \frac{(1.2+1)(5+0.6)}{20} = 0.62$$

To avoid core saturation during normal operation, primary inductance must be a minimum value determined by core volume and core flux density:

$$L_{PRI} \geq \left[\frac{V_{OUT} + V_F}{(N)(B_M)(f)}\right]^2 \left[\frac{(0.4\pi)(\mu_e)}{(V_e)(10^{-8})}\right]$$

B_M = maximum operating flux density
f = LT1070 operating frequency (40kHz)
V_e = core volume
μ_e = effective core permeability

Forward Converter



For B_M = 2000 gauss (typical for ferrites), V_e = 6cm^3, and μ_e = 1500, $V_{OUT} + V_F$ = 5.6V, N = 0.62:

$$L_{PRI} \geq \left[\frac{5.6}{(0.62)(2000)(40 \bullet 10^3)}\right]^2 \left[\frac{(0.4\pi)(1500)}{(6)(10^{-8})}\right]$$

$$= 400\mu H$$

The operating flux density of forward converters is often limited by temperature rise rather than saturation. At 2000 gauss, the core loss of a typical ferrite is 0.25W/cm^3. Total core loss at V_e = 6cm^3 ≈ 1.5W. When this is combined with copper winding losses, there may be excess core temperatures. Larger cores will allow more space for copper, or can be operated at lower flux density with the same copper loss. See Transformer Design guide for further details.

Conventional forward converters use a flip-flop to limit maximum duty cycle to 50% and set M = 1. The LT1070 will let duty cycle go to ≈95% during start-up and low input voltage conditions. This would cause core saturation and subsequent primary and switch currents of up to 10A. To avoid this, Q1 and R5 have been added. Onset of core saturation will cause a voltage drop across R5 high enough to turn on Q1 at each cycle. This pulls down on the V_C pin, reducing duty cycle and maintaining normal switch currents. R6 and C4 filter out spikes.

Operating duty cycle is given by:

$$DC = \frac{V_{OUT} + V_F}{(N)(V_{IN})}$$

The output filter inductor (L1) is chosen as a trade-off between maximum output power, output ripple, physical size and loop transient response. A reasonable value is one which gives a peak-to-peak inductor ripple current (ΔI_L) of ≈20% of I_{OUT}. This leads to a value for L1 of:

$$L1 = \frac{V_{OUT}\left[(N)(V_{IN}) - V_{OUT}\right]}{\left[(0.2)(I_{OUT})\right]\left[(N)(V_{IN})(f)\right]}$$

for I_{OUT} = 6A, V_{IN} = 25V, V_{OUT} = 5V, N = 0.62:

$$L1 = \frac{5\left[(0.62)(25) - 5\right]}{\left[(0.2)(6)\right]\left[(0.62)(25)(40 \bullet 10^3)\right]} = 70\mu H$$

Larger values of L1 will increase maximum output current only slightly. Output ripple voltage will go down inversely with larger L1, but physical size will quickly become a problem for large values because the inductor must handle large DC currents. Peak inductor current is equal to $I_{OUT} + \Delta I_L/2$.

Maximum output current for this forward converter is given by:

$$I_{OUT(MAX)} = \left(\frac{I_P}{N} - \frac{\Delta I_L}{2} - \frac{\Delta I_{PRI}}{N}\right)(0.9)$$

I_P = maximum LT1070 switch current
ΔI_{PRI} = peak primary magnetizing current
= $V_{OUT}/(f)(N)(L_{PRI})$
ΔI_L = peak-to-peak output inductor current
0.9 = fudge factor for losses

For I_P = 5A, N = 0.62, ΔI_L = 1.2A, ΔI_{PRI} = 0.5A;

$$I_{OUT(MAX)} = \left(\frac{5}{0.62} - \frac{1.2}{2} - \frac{0.5}{0.62}\right)(0.9) = 6A$$

Output voltage ripple (P-P) is assumed to be set by L1 and the ESR of C1:

$$V_{P\text{-}P} = (\Delta I_L)(ESR1) = \frac{ESR1(V_{OUT})\left[N(V_{IN}) - V_{OUT}\right]}{(L1)(f)(N)(V_{IN})}$$

ESR1 = effective series resistance of C1

If we assume 0.02Ω for ESR1, and V_{IN} = 25V,

$$V_{P\text{-}P} = \frac{(0.02)(5)\left[(0.62)(25) - 5\right]}{(70 \bullet 10^{-6})(40 \bullet 10^3)(0.62)(25)}$$

$$= 24mV_{P\text{-}P}$$

If less output ripple is desired, the most effective method may be to add an LC filter. See section on Output Filters.

FREQUENCY COMPENSATION

Although the architecture of the LT1070 is simple enough to lend itself to a mathematical approach to frequency compensation, the added complication of input and/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage and load current variations all suggest a more practical empirical method. Many hours spent on breadboards have shown that the simplest way to optimize the frequency compensation of the LT1070 is to use transient response techniques and an "R/C box" to quickly iterate toward the final compensation network.

There are many ways to inject a transient signal into a switching regulator, but the suggested method is to use an AC coupled output load variation. This technique avoids problems of injection point loading and is general to all switching topologies. The only variation required may be an amplitude adjustment to maintain small signal conditions with adequate signal strength. Figure 32 shows the setup.

A function generator with 50Ω output impedance is coupled through a 50Ω/1000µF series RC network to the regulator output. Generator frequency is noncritical. A good starting point is ≈50Hz. Lower frequencies may cause a blinking scope display which is annoying to work with. Higher frequencies may not allow sufficient settling time for the output transient. Amplitude of the generator output is typically set at $5V_{P-P}$ to generate a $100mA_{P-P}$ load variation. For lightly loaded outputs (I_{OUT} < 100mA), this level may be too high for small signal response. If the positive and negative transition settling waveforms are significantly different, amplitude should be reduced. Actual *amplitude* is not particularly important because it is the *shape* of the resulting regulator output waveform which indicates loop stability.

A 2-pole oscilloscope filter with f = 100kHz is used to block switching frequencies. Regulators without added LC output filters have switching frequency signals at their outputs which may be much higher amplitude than the low frequency settling waveform to be studied. The filter frequency is high enough to pass the settling waveform with no distortion.

Oscilloscope and generator connections should be made exactly as shown to prevent ground loop errors. The oscilloscope is sync'd by connecting channel "B" probe to the generator output, with the ground clip of the second probe connected to exactly the same place as channel "A" ground. The standard 50Ω BNC sync output of the generator should *not* be used because of ground loop errors. It may also be necessary to isolate *either* the generator or oscilloscope from its third wire (earth ground) connection in the power plug to prevent ground loop errors in the 'scope display. These ground loop errors are checked by connecting channel "A" probe tip to exactly the same point as the probe ground clip. Any reading on channel "A" indicates a ground loop problem.

Once the proper setup is made, finding the optimum values for the frequency compensation network is fairly straightforward. Initially, C2 is made large (≥2µF) and R3 is made small (≈1k). This nearly always ensures that the regulator will be stable enough to start iteration. Now, if the regulator output waveform is single-pole overdamped, (see the waveforms in Figure 33) the value of C2 is *reduced* in steps of about 2:1 until the response becomes slightly underdamped. Next, R3 is *increased* in steps of 2:1 to introduce a loop "zero." This will normally improve damping and allow the value of C2 to be further reduced. Shifting back and forth between R3 and C2 variations will now allow one to quickly find optimum values.

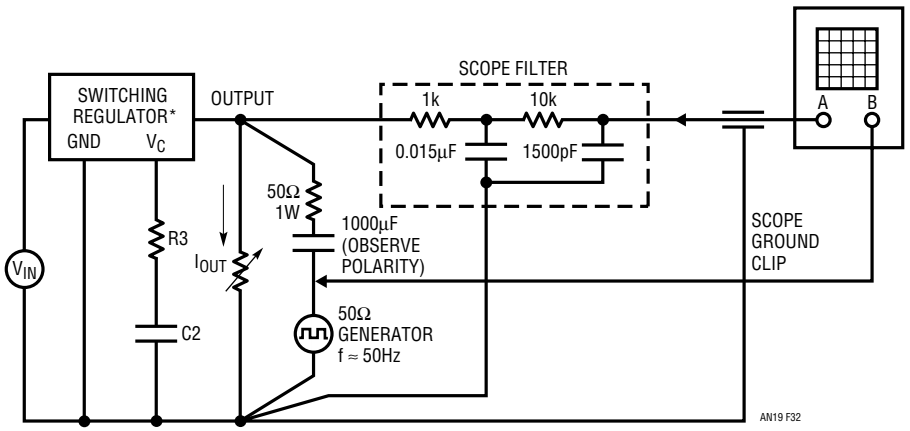
If the regulator response is underdamped with the initial large value of C, R should be increased immediately before larger values of C are tried. This will normally bring about the overdamped starting condition for further iteration.

Just what is meant by "optimum values" for R3 and C2? This normally means the smallest value for C2 and the largest value for R3 which still guarantee no loop oscillations, and which result in loop settling that is as rapid as possible. The reason for this approach is that it minimizes the variations in output voltage caused by *input ripple voltage* and *output load transients*. A switching regulator which is grossly overdamped will never oscillate, but it may have unacceptably large output transients following sudden changes in input voltage or output loading. It may

also suffer from excessive overshoot problems on start-up or short circuit recovery.

To guarantee acceptable loop stability under all conditions, the initial values chosen for R3 and C2 should be checked under all conditions of input voltage and load current. The simplest way of accomplishing this is to apply load currents of minimum, maximum and several points in between. At each load current, input voltage is varied from minimum to maximum while observing the settling waveform. The additional time spent "worst-casing" in this manner is definitely necessary. Switching regulators, unlike linear regulators, have large shifts in loop gain and phase with operating conditions.

If large temperature variations are expected for the regulator, stability checks should also be done at the temperature extremes. There can be significant temperature varia-



*ALL INPUT AND OUTPUT FILTERS MUST BE IN PLACE. INPUT SOURCE (V_{IN}) MUST BE ACTUAL SOURCE USED IN FINAL DESIGN TO ACCOUNT FOR FINITE SOURCE IMPEDANCE

Figure 32. Testing Loop Stability

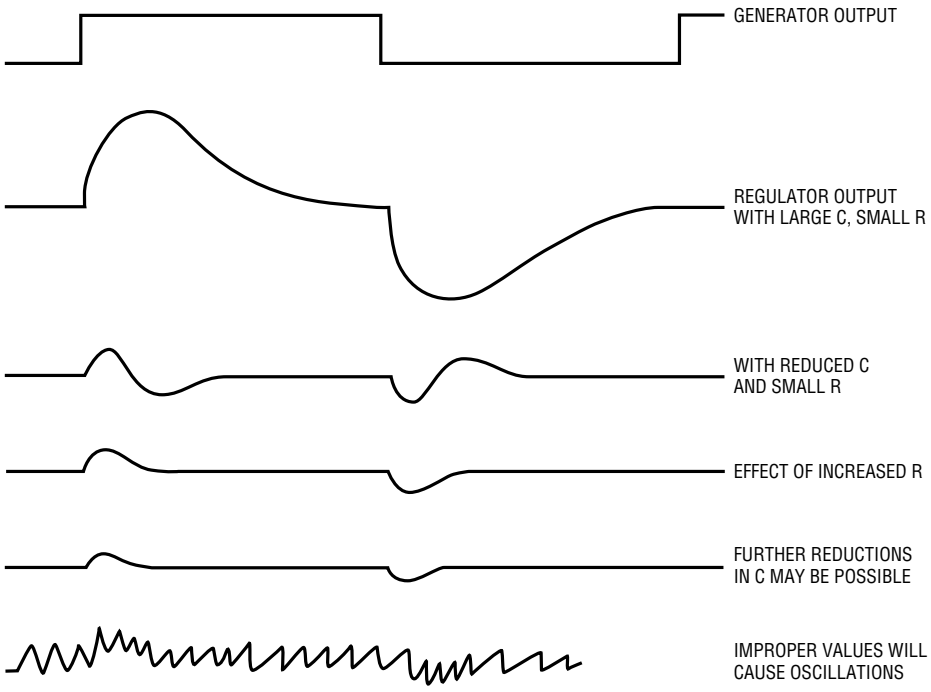


Figure 33. Output Transient Response

tions in several key component parameters which affect stability; in particular, input and output capacitor value and their ESR and inductor permeability. LT1070 parametric variations also need some consideration. Those which affect loop stability are error amplifier g_m and the transfer function of V_C pin voltage *versus* switch current (listed as a transconductance under electrical specifications). For modest temperature variations, conservative overdamping under worst-case room temperature conditions is usually sufficient to guarantee adequate stability at all temperatures.

Check Margins

One measure of stability "margin" is to vary the selected values of both R and C by 2:1 in all possible combinations. If the regulator response remains reasonably well damped under all line and load conditions, the regulator can be considered fairly tolerant of parametric variations. Any tendency towards an underdamped (ringing) response indicates that a more conservative compensation may be needed.

There are several large signal dynamic tests which should also be done on a completed regulator design. The first is to check response to the worst-case large amplitude load variation. A sudden change from light load to full load current may cause the regulator to have an unacceptably large transient dip in output voltage. The simplest cure for this is to increase the size of the output capacitor. Lower inductor values and less conservative frequency compensation also help. A second consideration is the output overshoot created when a large load is suddenly *removed*. This is potentially more dangerous than a dip because a large overshoot may destroy loads still connected to the regulator output.

Eliminating Start-Up Overshoot

Another transient condition to be checked is *start-up overshoot*. When input voltage is first applied to a switching regulator, the regulator dumps full short-circuit current into the output capacitor attempting to bring the output up to its regulated value. The output can then overshoot well beyond its design value before the control loop is able to idle back the output current. The amplitude of the overshoot can be anywhere from millivolts to tens of volts depending on topology, line and load conditions and component values. This same overshoot possibility exists for output recovery from output shorts. Again, larger output capacitors, smaller inductors and faster loop response help reduce overshoot. There are also several ways to force slow start-up to eliminate the overshoot. The first is to put a capacitor across the output voltage divider. This creates a time-dependent output voltage setting during start-up and usually eliminates overshoot. This capacitor also has an effect on feedback loop characteristics during normal operation and it can create unacceptably large negative transients on the feedback pin if the output voltage is high and a sudden output short occurs. The transient problem is eliminated by inserting a resistor in series with the feedback pin (see Feedback Pin part of Pin Description section). If undesirable loop characteristics are created by the capacitor, they can be eliminated by diode coupling the capacitor as shown in Figure 34.

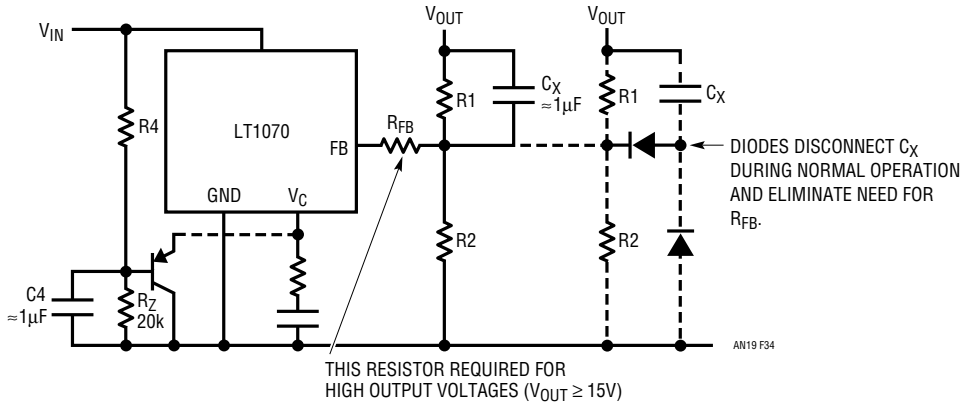


Figure 34. Eliminating Start-Up Overshoot

Another general technique for forcing slow start-up is to clamp the V_C pin to a capacitor, C4. The value of R4 is chosen to give a voltage across R_Z of 2V at worst-case *low* input voltage (I_{R4} = 100µA). C4 is then selected to ramp V_C slow enough to eliminate start-up overshoot. C4 should be made no larger than necessary to prevent long reset times. A momentary drop to zero volts at the input may not allow enough time for C4 to discharge fully. If input dropouts of less than 5R4C4 seconds are anticipated, R4 should be paralleled with a diode (cathode to input) for fast reset.

EXTERNAL CURRENT LIMITING

The LT1070 has internal *switch* current limiting which operates on a cycle-by-cycle basis and limits peak switch current to ≈9A at low duty cycles and ≈6A at high duty cycles. The actual *output* current limit value may be much *higher or lower* depending on topology, input voltage and output voltage. The following formulas give an approximate value for output current limit under short-circuit output conditions and at the point where output voltage just begins to fall below its regulated value.

	OVERLOAD CURRENT (AMPS)	SHORT CIRCUIT CURRENT (AMPS)
Buck	5 to 8	≈8
Boost	$(5\text{ to }8)(V_{IN}/V_{OUT})$	Not Allowed
Buck-Boost (Inverting)	$\frac{5\text{ to }8}{(1+V_{OUT}/V_{IN})}$	≈8
Current-Boosted Buck	$(5\text{ to }8)\left(\frac{V_{IN}}{V_{OUT}+N(V_{IN}-V_{OUT})}\right)$	≈8/N
Voltage-Boosted Boost	$(5\text{ to }8)\left(\frac{V_{IN}}{V_{OUT}+N(V_{IN})}\right)$	Not Allowed
Flyback (Continuous)	$\frac{5\text{ to }8}{(V_{OUT}/V_{IN})+N}$	≈8/N
Flyback (Discontinuous)	Depends on L	≈8/N
Current-Boosted Boost	$\frac{5\text{ to }8}{(V_{OUT}/V_{IN})-(N/N+1)}$	Not Allowed
Forward	5 to 8/N	≈8/N

These formulas show that short-circuit current can be much higher than full load current for some topologies. If either full load current or short circuit is much higher than is required for a specific application, external current limiting can be added. This has the advantage of reducing stress on external components, avoiding overload on the input supply and reducing heat sink requirements on the LT1070 itself.

The LT1070 is externally current limited by clamping the V_C pin. The techniques shown in Figures 35 to 39 are just a few of the ways this can be accomplished.

The relationship between *switch* current limit point and V_C clamp voltage is *approximately:*

$I_{SW(MAX)} = 9\ (V_C - 1) - 3 \bullet (DC)$ amps

DC = switch duty cycle

This relationship is somewhat temperature dependent. The current limit point falls at about 0.3%/°C, so the value set at room temperature should be factored to allow for adequate current limit at higher temperatures. Also, the factor "9" and "3" vary ±30% in production, so a conservative design will normally clamp switch current to about twice the value needed for maximum load current. This can result in rather high short-circuit currents, so the current limit scheme may want to include "foldback," wherein the peak switch current is clamped to a lower value with V_{OUT} = 0V. By varying the amount of foldback, the short-circuit current can be made greater than, equal to, or less than full load current.

Simple current limiting is shown in Figure 35. V_X is an external voltage which could be a separate regulated voltage or the unregulated input voltage. R2 is selected to give approximately 2V across R1. The value of R1 is kept to 500Ω or below to keep the knee of the current limit as sharp as possible. If individual adjustment is not necessary, R1 can be replaced with a fixed resistor. (Note that in some topologies the ground, V_C and FB pins of the LT1070 are switching at high voltage levels. This will require V_X to be referenced to the LT1070 ground pin, not system ground.)

In Figure 36, D1 has been replaced with a PNP transistor to reduce the current drain through R1 to 100µA. This is helpful in situations where the LT1070 is used in the total shutdown mode.

In Figure 37, *foldback* current limiting is generated by clamping the V_C pin to an output voltage divider. This will reduce short-circuit current by an amount which depends on the relative values of R3, R4 and R5. R5 is needed to prevent "latch off," wherein the output current drops to zero during short circuit and stays at zero even if the short is removed. If this latch-off action is desirable, R5 can be eliminated. A normally closed "start" switch can then be placed in series with D1. If *nonzero* short-circuit current is desired, R5 is selected to give desired short-circuit current and R4 is adjusted for full load current limit. There is some interaction, so R4 should be set to about midspan for initial selection of R5. If less interaction is desired between R4 and R5 adjustments, a 470Ω resistor can be inserted in series with the wiper on R4 to form a voltage divider with R5.

A current transformer (T1) is used in Figure 38 to generate a more precise current limit. The primary is placed in series with the output switching diode for buck, flyback and buck/boost configurations. Output diode *peak* current is limited to:

$$I_{PEAK} = \frac{N}{R5}\left(V_{BE} + \frac{V_{OUT} \bullet R4}{R3 + R4}\right)$$

V_{BE} = base-emitter voltage of Q1

The R3/R4 divider provides foldback as shown in the formula, with short-circuit diode current limited to $N(V_{BE}/R5)$. In a typical application, R3 is selected to set the voltage across R4 to ≈1V at normal output voltage. Then R5 is calculated from:

$$R5 = \frac{N\left(V_{BE} + V_{R4}\right)}{I_{PEAK(PRI)}}$$

The effective *secondary* current limit sense voltage is V_{BE} + V_{R4} at full output voltage and just V_{BE} during short circuit, giving ≈2.7:1 foldback ratio. The diode in T1 secondary allows the secondary to "reset" between current pulses, so that true peak-to-peak diode current is controlled. C1 is used to filter out spikes and noise.

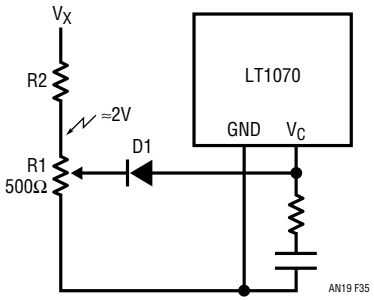


Figure 35. External Current Limit

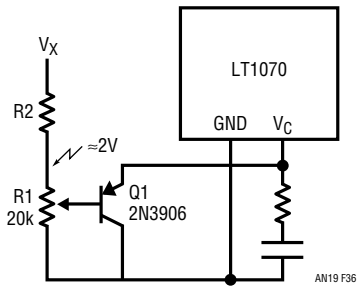


Figure 36. External Current Limit

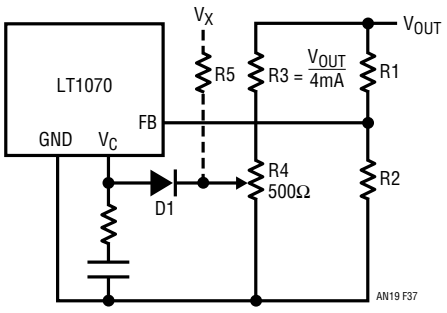


Figure 37. Foldback Current Limit

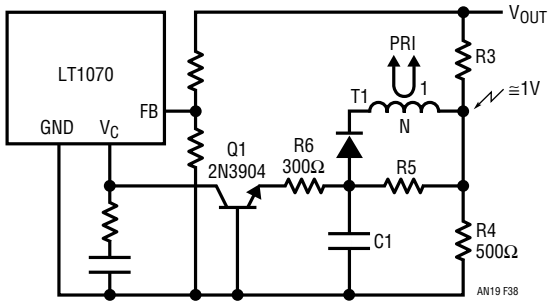


Figure 38. Transformer Current Limit

In Figure 39 a current limit sense resistor (R_S) is placed in series with the ground pin of the LT1070. Peak *switch* current is limited to $V_{BE}(Q1)/R_S$. This circuit is useful only in situations where the negative input line and the negative output line do not have to be common. Power dissipation in R_S will be fairly high; $P \approx (0.6V)(I_{PEAK})(DC)$, where DC is the duty cycle of the switch. R1 and C1 filter out noise spikes and catch diode reverse turn-off current spikes.

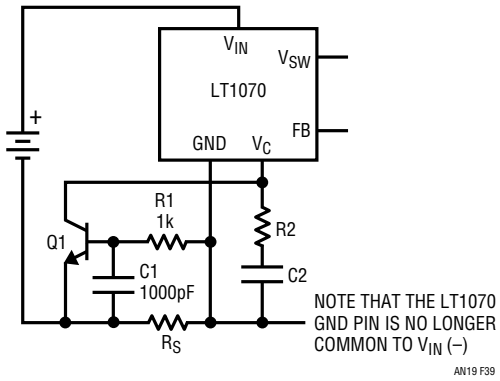


Figure 39. External Current Limit

DRIVING EXTERNAL TRANSISTORS

High input voltage applications using the LT1070 require an external high voltage transistor. The transistor is connected in a common gate or common base mode as shown in Figures 40 and 41. This allows the LT1070 internal current sensing to continue functioning and operates the external transistor in a mode which maximizes both operating voltage and switching speed capability.

In Figure 40, the LT1070 drives an N-channel power MOSFET. A separate low voltage supply is used to power the LT1070 and to establish forward gate drive to the MOSFET. Typical gate drive requirement is 10V, with 20V as a typical maximum. The forward gate drive applied to the MOSFET is equal to the supply voltage minus the saturation voltage of the LT1070 switch (saturation voltage is typically under 1V). D1 is used to clamp the source during turn-off; it does not slow down turn-off. Diode requirements are that it withstand narrow (100ns) current spikes equal to drain current and that it turn "on" rapidly to provide proper clamping.

In Figure 41, the LT1070 drives an NPN bipolar transistor. These devices require high surge base currents at turn-on and turn-off to ensure fast switching times. R1 establishes DC base drive which might be ≈1/5 of collector current. C1 provides a forward base current surge at turn-on. Typical values are in the range of 0.005µF to 0.05µF. D1 clamps the emitter voltage at turn-off. It prevents full collector current from flowing out the base lead during the turn-off delay time (0.5µs to 2µs). D2 and R1 establish the reverse base turn-off current. The voltage across R2 during turn-off delay time is approximately one diode drop. With R2 = 3Ω and a diode drop of 800mV, this would create ≈270mA reverse base current during turn-off. Reverse leakage in the "off" state is not a problem with this circuit because D1 and D2 force the emitter-base voltage to zero bias when the LT1070 switch is off. D1 should be selected for fast turn-on. It must handle current equal to collector current for times equal to the turn-off time of the transistor. D2 can be any medium speed diode rated for several hundred milliamps forward current spikes (1N914, etc.).

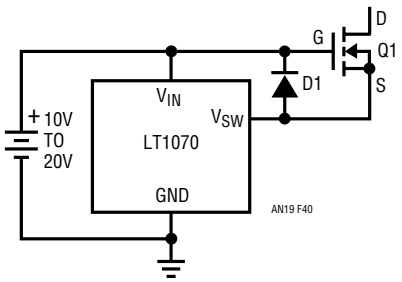


Figure 40. Driving External MOSFET

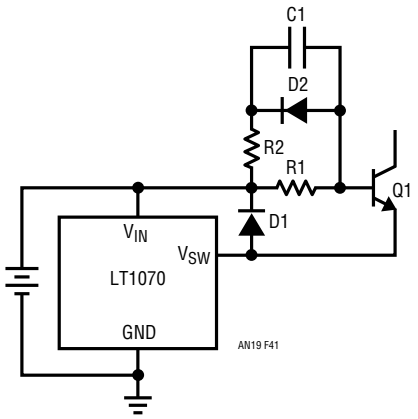


Figure 41. Driving External NPN

OUTPUT RECTIFYING DIODE

The output diode is often the major source of power loss in switching regulators, especially with output voltages below 10V. It is therefore very important to be able to calculate diode peak current and average power dissipation to ensure adequate diode ratings. The chart in Figure 42 lists average diode power dissipation and peak diode current for normal loads. It also lists diode current under shorted output conditions where the diode duty cycle approaches 100%, and peak and average currents are essentially the same.

The value for diode forward voltage (V_F) used in the average power formulas is the voltage specified for the diode under peak current conditions listed in the next column. The peak current formulas assume no ripple current in the inductor or transformer, but average power calculations will be reasonably close even with fairly high ripple. Boost converters in particular are hard on output diodes when the output voltage is significantly higher than the input voltage. This gives peak diode currents much higher than the average, and manufacturers current ratings must be used with caution.

The most stressful condition for output diodes is overload or short-circuit conditions. The internal current limit of the LT1070 is typically 9A at low switch duty cycles. This is almost a factor of two higher than the 5A rated switch current, so that even if the regulator is used near its limit at full load, the output diode current may double under current limit conditions. If full load output current requires only a fraction of the 5A rated switch current, the ratio of diode short-circuit current to full load current may be much higher than two to one. A regulator designed to withstand continuous short conditions must either use diodes rated for the full short-circuit current shown in the fourth column, or it must incorporate some form of external current limiting. See Current Limit section for more details.

The last column in Figure 42 shows maximum reverse diode voltage. When calculating this number, be sure to

TOPOLOGY	AVERAGE DIODE DISSIPATION P_D (WATTS)	PEAK DIODE CURRENT		PEAK DIODE VOLTAGE
		AT FULL LOAD (AMPS)	SHORT CIRCUIT (AMPS)	
Buck	$(I_{OUT})(V_F)(1-V_{OUT}/V_{IN})$	$I_{OUT}+\frac{\Delta I}{2}$	≈8	V_{IN}
Current-Boosted Buck	$(I_{OUT})(V_F)(1-V_{OUT}/V_{IN})$	$\frac{I_{OUT}}{V_{IN}}\left(\frac{V_{OUT}}{N}-V_{OUT}+V_{IN}\right)$	≈8/N	$V_{OUT}+N(V_{IN})$
Boost	$(I_{OUT})(V_F)$	$\frac{I_{OUT}(V_{OUT})}{V_{IN}}+\frac{\Delta I}{2}$	Not Allowed	V_{OUT}
Current-Boosted Boost	$(I_{OUT})(V_F)$	$I_{OUT}\left[\frac{V_{OUT}}{V_{IN}}+N\left(\frac{V_{OUT}}{V_{IN}}-1\right)\right]+\frac{\Delta I_{PRI}(N+1)}{2}$	Not Allowed	$V_{OUT}-V_{IN}\left(\frac{N}{N+1}\right)$
Voltage-Boosted Boost	$(I_{OUT})(V_F)$	$\frac{I_{OUT}(N\bullet V_{IN}+V_{OUT})}{V_{IN}(N+1)}$	Not Allowed	$V_{OUT}+N(V_{IN})$
Inverting (Buck Boost)	$(I_{OUT})(V_F)$	$\frac{I_{OUT}(V_{IN}+V_{OUT})}{V_{IN}}+\frac{\Delta I}{2}$	≈8	$V_{OUT}+V_{IN}$
Flyback (Continuous)	$(I_{OUT})(V_F)$	$I_{OUT}\left(1+\frac{V_{OUT}}{N(V_{IN})}\right)+\frac{\Delta I_{PRI}}{2N}$	≈7/N	$V_{OUT}+N(V_{IN})$
Flyback (Discontinuous)	$(I_{OUT})(V_F)$	$\frac{1}{N}\sqrt{\frac{2(I_{OUT})(V_{OUT})}{f(L_{PRI})}}$	≈7/N	$V_{OUT}+N(V_{IN})$

AN19 F42

Figure 42

use worst-case high input voltage. Transformer or tapped inductor designs may have an additional damped "ringing" waveform which adds to peak diode voltage. This can be reduced with a series R/C damper network in parallel with the diode.

Switching diodes have two important transient characteristics: reverse recovery time and forward turn-on time. Reverse recovery time occurs because the diode "stores" charge during its forward conducting cycle. This stored charge causes the diode to act like a low impedance conductive element for a short period of time after reverse drive is applied. Reverse recovery time is measured by forward biasing the diode with a specified current, then forcing a second specified current *backwards* through the diode. The time required for the diode to change from a reverse *conducting* state to its normal reverse *nonconducting* state, is reverse recovery time. Hard turn-off diodes switch abruptly from one state to the other following reverse recovery time. They, therefore, dissipate very little power even with moderate reverse recovery times. Soft turn-off diodes have a gradual turn-off characteristic that can cause considerable diode dissipation during the turn-off interval. Figure 43 shows typical current and voltage waveforms for several commercial diode types used in an LT1070 boost converter with V_{IN} = 10V, V_{OUT} = 20V, 2A.

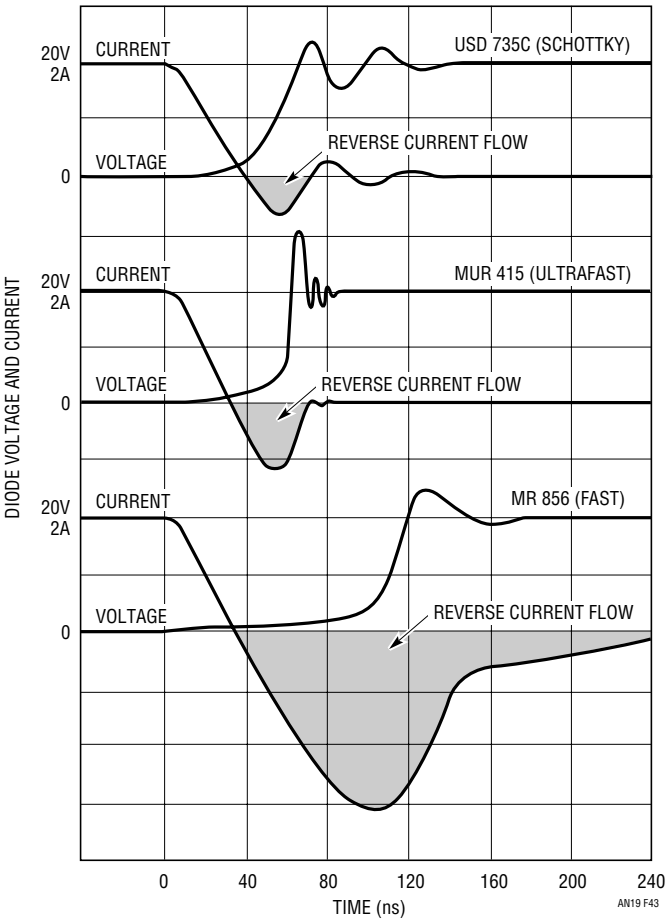


Figure 43. Diode Turn-Off Characteristics

Long reverse recovery times can cause significant extra heating in the diode or the LT1070 switch. Total power dissipated is given by:

$$P_{tRR} = (V)(f)(t_{RR})(I_F)$$

V = reverse diode voltage
f = LT1070 switching frequency
t_{RR} = reverse recovery time
I_F = diode forward current just prior to turn-off

With the circuit mentioned, I_F is 4A, V = 20V and f = 40kHz. Note that diode "on" current is twice output current for this particular boost configuration. A diode with t_{RR} = 300ns creates a power loss of:

$$P_{tRR} = (20)(40 \bullet 10^3)(300 \bullet 10^{-6})(4) = 0.96W$$

If this same diode had a forward voltage of 0.8V at 4A, its forward loss would be 2A (*average* current) times 0.8V equals 1.6W. Reverse recovery losses in this example are nearly as large as forward losses. It is important to realize, however, that reverse losses may not necessarily increase *diode* dissipation significantly. A hard turn-off diode will shift much of the power dissipation to the LT1070 switch, which will undergo a high current *and* high voltage condition during the duration of reverse recovery time. This has not shown to be harmful to the LT1070, but the power loss remains.

Diode *turn-on* time can potentially be more harmful than reverse turn-off. It is normally assumed that the output diode clamps to the output voltage and prevents the inductor or transformer connection from rising higher than the output. A diode that turns "on" slowly can have a very high forward voltage for the duration of turn-on time. The problem is that this increased voltage appears across the LT1070 switch. A 20V turn-on spike superimposed on a 40V boost mode output pushes switch voltage

perilously close to the 65V limit. The graphs in Figure 44 show diode turn-on spikes for three common diode types, fast, ultrafast and Schottky. The height of the spike will be dependent on rate of rise of current and the final current value, but these graphs emphasize the need for fast turn-on characteristics in applications which push the limits of switch voltage.

Fast diodes can be useless if the stray inductance is high in the diode, output capacitor or LT1070 loop. 20-gauge hookup wire has ≈30nH/inch inductance. The current fall time of the LT1070 switch is $\approx 10^8$A/sec. This generates a voltage of $(10^8)(30 \bullet 10^{-9})$ = *3V per inch* in stray wiring. Keep the diode, capacitor and LT1070 ground/switch lead lengths *short*.

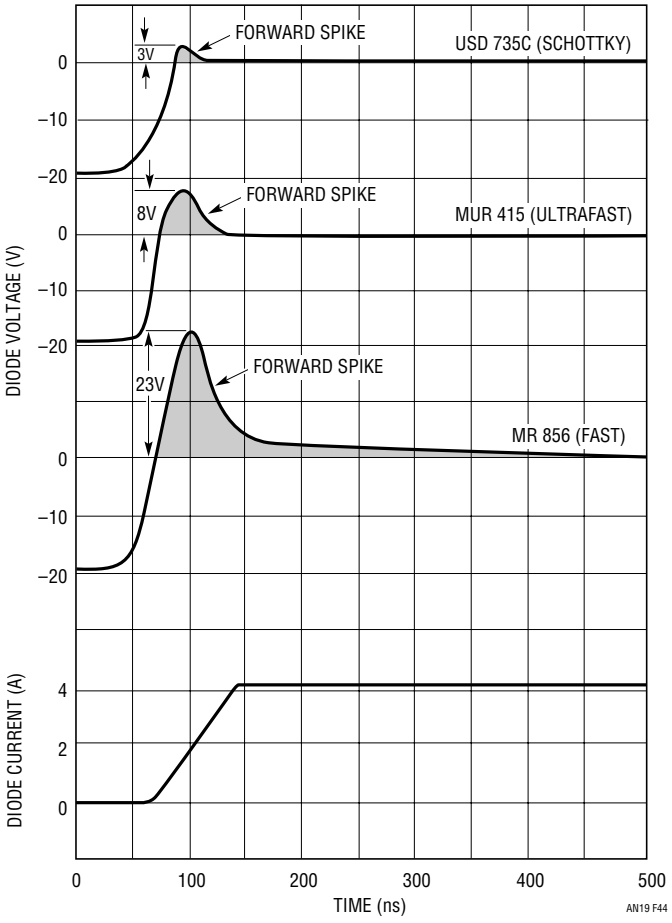


Figure 44. Diode Turn-On Spike

INPUT FILTERS

Most switching regulator designs draw current from the input supply in pulses. The peak-to-peak amplitude of these current pulses is often equal to or higher than the load current. There is significant high frequency energy in the pulses which can cause EMI problems in some systems. The addition of a simple LC filter between the supply and the switching regulator can reduce the amplitude of this EMI by more than an order of magnitude at the switching frequency and several orders of magnitude at higher harmonic frequencies. The basic filter shown in Figure 45 can be added to any switching regulator.

The two major design considerations for the filter are the *reverse current transfer function* which determines ripple attenuation and the *filter output impedance function* which must satisfy regulator stability criteria. The stability problem occurs because switching regulators have a *negative input impedance* at low frequencies:

$$Z_{IN}(DC) = -\frac{(V_{IN})^2}{(V_{OUT})(I_{OUT})}$$

The output impedance of the filter has a sharp peak at the LC resonant frequency. If the output impedance is not well below the negative input impedance of the regulator at frequencies up to the bandwidth of the regulator control loop, the possibility for oscillation exists.

There is a basic conflict in the two filter requirements. High ripple attenuation is obtained with a large LC *product* with high Q, but this also tends to aggravate oscillation problems. This conflict is minimized by using large C with smaller L to get the required LC product, but size requirements may also limit this approach. An additional "fix" is to lower the Q of the filter by paralleling L with a small

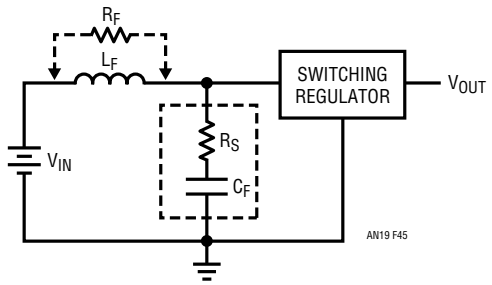


Figure 45

resistor (R_F). This has the disadvantage of limiting the filter attenuation at high frequencies. Filter Q is also reduced by the ESR (R_S) of the capacitor, but deliberately increasing ESR exacts a heavy penalty in ripple attenuation and power loss.

Ripple attenuation of an input filter may be calculated from:

$$\frac{I_{OUT(P-P)}}{I_{IN(P-P)}} = \frac{R_S}{R_F} + \frac{R_S(DC)(1-DC)}{(L)(f)}$$

R_S = effective series resistance of C
DC = switching regulator duty cycle

Note that this formula does not contain the value of C. This is because large electrolytic capacitors have a total impedance at 20kHz and above which is essentially equal to ESR. For ripple attenuation, therefore, the value of C is not important; the capacitor is selected on the basis of its ESR.

A typical filter might consist of a 10µH inductor and a 500µF capacitor with $R_S = 0.05\Omega$. Filter attenuation is *least effective* at 50% duty cycle (DC = 0.5), so we will use this number now for worst-case purposes. Ripple attenuation of this filter with $R_F = \infty$ is:

$$\frac{I_{OUT}}{I_{IN}} = \frac{(0.05)(0.5)(1-0.5)}{(10 \bullet 10^{-6})(40 \bullet 10^{3})} = 0.031 = 32{:}1$$

The formula assumes rectangular wave inputs with triangular outputs and yields the ratio of peak-to-peak values. Higher frequency components of the square wave current are attenuated much more than the overall attenuation figure.

Output impedance of the filter given by:

$$Z_{OUT} = \frac{1}{\frac{1}{R_F} - \frac{J}{\omega L} + \frac{J\omega C}{1+(\omega R_S C)^2} + \frac{R_S(\omega C)^2}{1+(\omega R_S C)^2}}$$

ω = radian frequency = $2\pi(f)$

This formula has a DC ($\omega = 0$) value of zero and a high frequency value equal to R_S in parallel with R_F. If R_S is simply the ESR of the capacitor, both high and low frequency output impedance of the filter is very low. Unfortunately, the output impedance of the filter at its resonant frequency can be significantly higher, and this resonant frequency is typically in the range where switching regulators have negative input impedance. Resonant frequency and peak output impedance formulas are shown below.

$$f = \frac{1}{2\pi\sqrt{LC - (R_S)^2(C)^2}}$$

If R_S is simply the ESR of C, the filter resonant frequency is usually closely approximated by:

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad \left[\frac{(R_S)^2(C)}{L} << 1\right]$$

$$Z_{OUT(PEAK)} = \frac{R_F(LC)}{LC + (R_S)(R_F)(C)^2}$$

Resonant frequency for a 500µF, 10µH filter is ≈2kHz. Peak output impedance with $R_F = \infty$ and $R_S = 0.05\Omega$ is ≈0.4Ω.

The criterion for regulator stability is that the filter impedance be much lower than the input impedance of the regulator:

$$\frac{R_F(LC)}{LC + (R_S)(R_F)(C)^2} << Z_{IN}$$

The worst case occurs with switching regulators that have low input voltage. If we let $V_{IN} = 5V$, and $V_{OUT} = 20V$, $I_{OUT} = 1A$, regulator input impedance at low frequencies is $(5^2)/(20)(1) = 1.25\Omega$. The peak filter impedance was calculated at 0.4Ω, so it seems that stability criterion is met. There is the problem, however, of the *too good* a capacitor in the filter. If the ESR of C drops to 0.02Ω, peak

filter impedance rises to 1Ω and stability becomes questionable. To bring peak filter impedance down, R_F may have to be added. If R_F is set at 1Ω, peak filter impedance drops to 0.5Ω. The penalty in ripple attenuation is a reduction from 32:1 to 12:1 for R_S = 0.05Ω.

In all this discussion, the output impedance of the actual input *source* was assumed to be zero. This is not the actual case obviously, and source impedance may have a significant effect on stability.

The point of all this is that input filters tend to have resonant frequencies and impedances which fall into the range where they can cause stability problems in switching regulators. It is important, therefore, to include the filter design into the overall regulator design from the beginning. The selected filter must be *in place* when the regulator is checked for closed-loop stability and the actual source should be used.

EFFICIENCY CALCULATIONS

The primary reason for using switching regulators is efficiency, so it is important to be able to estimate that factor with some degree of accuracy. In may cases, the overall efficiency is not as critical as the power loss in the individual components. For reliable operation, each power dissipating component must be properly sized or heat sunk to ensure that maximum operating temperature is not exceeded. Overall efficiency is then found by dividing output power by the sum of all losses plus output power:

$$E = \frac{(I_{OUT})(V_{OUT})}{\Sigma P_L + (I_{OUT})(V_{OUT})}$$

Sources of power loss include the LT1070 quiescent current, switch driver current and switch "on" resistance; the output diode; inductor/transformer winding and core losses; and snubber dissipation.

LT1070 Operating Current

The LT1070 draws only 6mA quiescent current in its idle state, but this is specified with a voltage on the V_C pin such that the output switch never turns on—duty cycle equals zero. When the V_C pin is servoed by the feedback loop to initiate switching, supply current at the input pin increases in two ways. First, there is a DC increase proportional to V_C pin voltage. This is the result of increasing bias current for the switch driver to ensure adequate switch drive at high switch currents. Second, there is driver current which is "on" only when the output switch is on. The ratio of switch driver current to switch current is ≈1:40. Total *average* current into the LT1070 V_{IN} pin is then:

$$I_{IN} \approx 6mA + I_{SW}(0.0015 + DC/40)$$

I_{SW} = switch current
DC = switch duty cycle

Use of this formula requires knowledge of switch duty cycle and switch current. This information is available in the sections that deal with each particular switching configuration. A typical example is a buck converter with 28V input and 5V, 4A output. Duty cycle is ≈20% and switch current is 4A. This yields a total supply current of:

$$I_{IN} = 6mA + 4(0.0015 + 0.2/40) = 32mA$$

Total power loss due to bias and driver current is equal to input voltage times current:

$$P_{BD} = (I_{IN})(V_{IN}) = (32mA)(28V) = 0.9W$$

LT1070 Switch Losses

Switch "on" resistance losses are proportional to the square of switch current multiplied times duty cycle:

$$P_{SW} = (I_{SW})^2 (R_{SW})(DC)$$

R_{SW} = LT1070 switch "on" resistance

The maximum specified value for R_{SW} is 0.24Ω at maximum rated junction temperature, with 0.15Ω typical value at room temperature. If we use the worst-case number of 0.24Ω, this yields a switch loss in this example of:

$$P_{SW} = (4)^2(0.24)(0.2) = 0.77W$$

It is pure coincidence that switch and driver losses are nearly equal in this example. At low switch currents and high input voltages, P_{BD} dominates, whereas switch losses dominate at low input voltages and high switch currents.

AC switching losses in the LT1070 are minimal. Rate of switch current rise and fall is $\approx 10^8$A/sec. This reduces switching times to under 50ns and makes the AC losses small compared to DC losses. An exception to this is the

AC switch loss attributable to output diode reverse recovery time. See Output Diode section.

Output Diode Losses

For low to moderate output voltages, the output diode is often the major source of power loss. For this reason, Schottky switching diodes are recommended for minimum forward voltage and reverse recovery time. Diode losses for most topologies can be approximated by the following formula, but please consult the Output Diode section for further details:

$$P_D \approx (I_{OUT})(V_F)(K) + (V)(f)(t_{RR})(I_F)$$

V_F = diode forward voltage at *peak* diode current
V = diode reverse voltage
t_{RR} = diode reverse recovery time
I_F = diode forward current at turn-off
$K = 1 - (V_{OUT}/V_{IN})$ for buck converters and 1 for most other topologies

In the buck regulator example, with I_{OUT} = 4A and letting V_F = 0.7V, t_{RR} = 100ns:

$$P_D = (4)(0.7)(1 - 5/28) + (28)(40 \bullet 10^3)(10^{-7})(4)$$
$$= 2.3 + 0.45 = 2.75W$$

Inductor and Transformer Losses

See section on Inductors and Transformers.

Snubber Losses

See section on Flyback design.

Total Losses

In this example of a buck regulator, inductor losses might be ≈1W and snubber losses are zero. Total losses therefore are:

$$\Sigma P_L = P_{BD} + P_{SW} + P_D + P_L + P_{SNUB}$$
$$= 0.9 + 0.77 + 2.75 + 1 + 0 = 5.42W$$

Efficiency is equal to:

$$E = \frac{(V_{OUT})(I_{OUT})}{\Sigma P_L + (V_{OUT})(I_{OUT})} = \frac{(5)(4)}{5.42 + (5)(4)} = 78.7\%$$

This number is typical of a fairly high efficiency 5V buck regulator. The efficiency of 5V switching supplies is lower than higher voltage outputs because of the high diode losses. A 15V output, for instance, might have E ≈ 86%.

OUTPUT FILTERS

Output voltage ripple of switching regulators is typically in the range of tens to hundreds of millivolts if no additional output filter is used. A simple output filter can reduce this ripple by a factor of ten to one hundred at little additional cost. The high frequency "spikes" which may be superimposed on the ripple are attenuated even more.

The presence of high amplitude spikes at the output of switching regulators is often puzzling to first time designers. These spikes occur in switching regulators which, by their topology, cannot use the energy storage inductor as an output filter. These include boost, flyback and buck/boost designs. The output of these converters can be modeled as a switched current source driving the output capacitor as shown in Figure 46.

The output capacitor is shown as C_{OUT}. Its model includes parasitic resistance (R_S) and inductance (L_S). It is the inductance which creates the output voltage spike. The amplitude of this spike can be calculated if the slew rate (dI/dT) of the switch is known. For simple inductor designs operating at full switch current, dI/dT for the

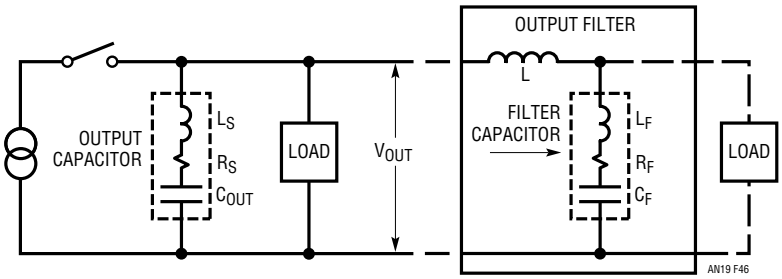


Figure 46. Output Filter

LT1070 switch is approximately 10^8A/sec. Voltage across L_S is:

$$V = L_S\left(\frac{dI}{dT}\right) = L_S\left(10^8\right)$$

Straight wire has an inductance of about 0.02µH per inch. If we assume one inch of wire on each end of the output capacitor, including board trace length, this represents 0.04µH. Allowing an additional 0.02µH *internal* inductance, L_S has a total value of 0.06µH, yielding:

$$V = \left(0.06\right)\left(10^{-6}\right)\left(10^8\right) = 6V$$

These spikes are very narrow (<100ns) and are usually attenuated significantly in the wire runs and load bypass capacitors, but these calculations point out the importance of s*hort lead lengths* on the output capacitor.

Output voltage ripple at the regulator switching frequency is usually of two types. With boost, flyback and inverting (buck/boost) designs, ripple is determined almost totally by the ESR of the output capacitor (R_S).

The *reactance* $1/(2\pi f_C)$, of the capacitor at 40kHz is normally so low compared to R_S that it can be ignored. The output ripple is therefore a square wave with amplitude V_{P-P} and duty cycle DC. A formula for V_{P-P} and DC is given in the discussions of these topologies.

The second type of output ripple is triangular. It occurs in switching regulators which utilize the storage inductor as an output filter. These include buck converters, forward converters and 'Cuk converters. Again, the amplitude of the ripple is determined by R_S, not C, but the waveform is triangular with amplitude V_{P-P} and duty cycle DC.

The attenuation of an output filter with *rectangular inputs* is:

$$\frac{V_{OUT(P-P)}}{V_{P-P}} = \frac{DC\left(1-DC\right)\left(R_F\right)}{\left(f\right)\left(L\right)}$$

$$DC = \text{duty cycle of rectangular inputs}\left(50\% = 0.5\right)$$

Notice that attenuation is the same for complementary duty cycles, that is 10% and 90% are equal, and 40% and 60% are equal, 50% is the point of poorest attenuation. A converter running at 40% duty cycle with an output filter consisting of a 10µH inductor and a 200µF capacitor with $R_F = 0.05\Omega$ would have a filter attenuation of:

$$\frac{V_{OUT(P-P)}}{V_{P-P}} = \frac{\left(0.4\right)\left(0.6\right)\left(0.05\right)}{\left(4\bullet10^3\right)\left(10\bullet10^{-6}\right)} = 0.03 = 33{:}1$$

The rectangular input is converted to a triangular output whose peak-to-peak amplitude is 1/33 of the peak-to-peak input. Harmonics of the switching frequency are reduced much more; the third harmonic for instance is attenuated 112:1 with $L_F = 0.06\mu H$. There are no second harmonics.

With buck, forward and 'Cuk converters, the ripple voltage into the filter is already triangular. The output ripple of the filter is of the form $V(t) = mt^2$. Attenuation ratio is given by:

$$\frac{V_{OUT(P-P)}}{V_{P-P}} = \frac{R_F}{\left(8\right)\left(L\right)\left(f\right)}$$

For the same conditions of $R_F = 0.05\Omega$, L = 10µH:

$$\frac{V_{OUT(P-P)}}{V_{P-P}} = \frac{0.05}{\left(8\right)\left(10\bullet10^{-6}\right)\left(40\bullet10^3\right)} = 0.0156 = 64{:}1$$

The ripple voltage of these converters is already lower because of the main inductor filtering, so the output filter inductor can often be only a few µH to obtain adequate filtering. The inductor can even be an air core type. A 1/2" diameter, 3/4" long air-wound coil with 13 turns of #16 wire will have an inductance of 1µH, giving a 6:1 attenuation with $R_F = 0.05\Omega$.

INPUT AND OUTPUT CAPACITORS

Large electrolytic capacitors used on switching regulators have several important design considerations. The most important is usually effective series resistance (ESR). This is simply the equivalent parasitic resistance in series with the capacitor leads. At frequencies of 10kHz and above, the total impedance of the capacitor is almost identically equal to ESR, and this parasitic resistance limits the filtering effectiveness of the capacitor. The design equations for capacitors used with the LT1070 most often deal

simply with ESR; the actual capacitance value is of secondary importance. The following formulas are a very rough guide to maximum ESR vs capacitance for several types of commercially available switching supply capacitors. ESR changes over temperature are shown in Figure 47.

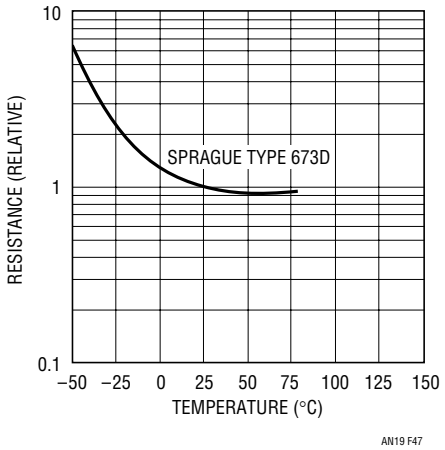


Figure 47. Typical Capacitor ESR vs Temperature

Sprague types 673D or 674D

$$ESR = \frac{(400)(10^{-6})}{(C)(V)^{0.6}}\Omega$$

Mallory type VPR

$$ESR = \frac{(200)(10^{-6})}{(C)(V)^{0.6}}\Omega$$

Cornell Dubilier Type UFT

$$ESR = \frac{(430)(10^{-6})}{(C)(V)^{0.25}}\Omega$$

C = capacitance value
V = rated working voltage

Note that higher voltage ratings yield lower ESR. This is because higher voltage capacitors are physically larger! Nothing's free, folks. Common design practice is to parallel several capacitors to achieve low ESR and acceptable component height.

A second consideration in capacitor selection is ripple current rating. After a capacitor has been selected, its ripple current rating should be checked to verify that operating ripple is less than the maximum allowed by the manufacturer. Keep in mind, however, that ripple current ratings are normally selected to limit temperature rise in the capacitor. Power dissipation is given by $(I_{RMS})^2(ESR)$. For ambient temperatures below the capacitor's maximum rating, it may be possible to increase ripple current. Consult the capacitor manufacturer. RMS ripple current in the output capacitor for boost, buck-boost and flyback designs can be calculated from output current and switch duty cycle:

$$I_{RMS} = I_{OUT}\sqrt{\frac{DC}{1-DC}}$$

For buck converters, RMS current in the output capacitor is approximately equal to $0.3\Delta I$, where ΔI is the peak-to-peak ripple current in the inductor (continuous mode).

Ripple current in the input capacitor for flyback and buck-boost designs is:

$$I_{RMS} = \frac{(I_{OUT})(V_{OUT})}{V_{IN}}\sqrt{\frac{1-DC}{DC}}$$

For buck designs it is:

$$I_{RMS} = I_{OUT}\sqrt{DC-(DC)^2}$$

and for boost designs, input capacitor ripple current is:

$$I_{RMS} = 0.3\Delta I$$

INDUCTOR AND TRANSFORMER BASICS

The inductors and transformers used with the LT1070 are very important to the overall performance of the converter, especially with respect to parameters such as efficiency, maximum output power and overall physical size. The many trade-offs associated with the inductance values and the volume of the core require the designer to have a sound basis for selecting the optimum inductor or trans-

former for each application. Specific guidelines for inductance values are given in the discussion of suggested applications elsewhere in this section, but a general understanding of inductor theory is also needed.

The three important characteristics of a simple 2-terminal inductor used in switching regulators are: inductance value (L, in henries), maximum energy storage ($I^2 \bullet L/2$, in ergs) and power loss (watts). Basic definitions of the parameters which determine these characteristics are shown below.

μ = core permeability. This is basically the *increase* in inductance which is obtained when the inductor is wound on a core instead of just air. A μ of 2000, for instance, will increase inductance by 2000:1.

ℓ = magnetic path length. In a simple toroid this is the average circumference of the core (see sketch).

A = cross-sectional area of the core (see sketch).

g = thickness of air gap (if any) used to increase the energy storage capability of a core (see sketch).

B = magnetic flux density in the core. If B rises too high, the core will "saturate," allowing μ and therefore L, to drop drastically.

N = number of turns in the winding.

I = instantaneous winding current.

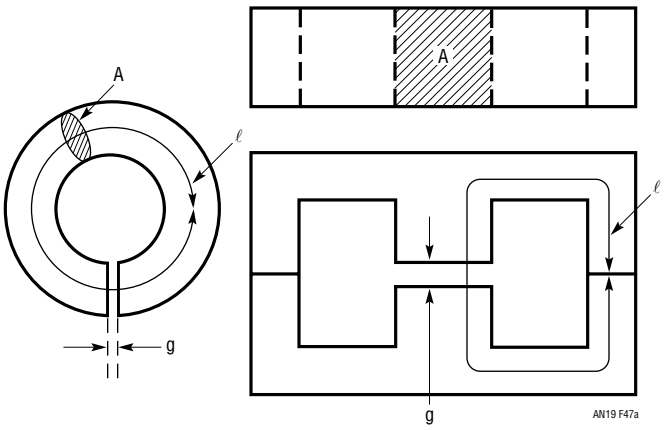
V_C = volume of actual core material.

In most converter applications, the required inductance is determined by constraints such as maximum output power, ripple requirements, input voltage and transient response. I is determined by load current. For purposes of this discussion, therefore, it is assumed that L and I are known quantities, and the quantities to be determined are N, A, ℓ, V_C and g.

Inductance is determined by core permeability, path length, cross sectional area and number of turns:

$$L = \frac{(\mu)(A)(N^2)}{\ell}(0.4\pi)(10^{-8}) \quad (\text{no gap})$$

Magnetic flux density is a function of winding current, number of turns and path length:



Toroid **E-E Core**

$$B = \frac{(I)(N)(\mu)}{\ell}(0.4\pi) \quad (\text{no gap})$$

A properly selected inductor must provide the right value of L without exceeding the maximum limit on flux density, (B_M). In other words, the core must not "saturate" under conditions of peak winding current (I_P). By combining the formulas for inductance and flux density, it can be shown that core *volume* (V_C) required is a direct function of the energy to be stored by the inductor:

$$\text{Stored energy} = E = \frac{(I_P{}^2)(L)}{2}$$

$$V_C = (A)(\ell) = \frac{(I_P{}^2)(L)(\mu)(0.4\pi)}{(B^2)(10^{-8})} = (E)\frac{(2\mu)(0.4\pi)}{(B^2)(10^{-8})}$$

In any given application, the value of I_P can be determined from maximum load current and duty cycle. Formulas for maximum I_P are provided in the individual sections on each topology.

In many cases, the maximum load current is much less than the LT1070 is capable of providing. A core designed to handle only full load current may saturate under overload or short-circuit conditions. The *cycle-by-cycle current limiting of the LT1070 protects the regulator against damage even with saturated cores*. This considerably

improves the reliability of converters using the LT1070 and eases the design complexity.

Although core volume is the main criterion for selecting a given core, the volume still consists of two variables, A and ℓ. For minimum overall size of the inductor it is generally best to increase A as much as possible at the expense of ℓ, thereby minimizing the number of turns required to obtain the desired inductance. This process can be taken only so far before the "window" in the core becomes too small to accommodate the windings.

Cores with Gaps

The energy storage capability of a core can be increased by "gapping" the core. A significant portion of the total energy is stored in the air gap. The drawback of a gapped core is that the effective permeability drops, requiring many more turns to achieve the required inductance. More turns require a larger winding window. The overall size of the inductor, however, can be considerably less with a properly gapped core, especially with high permeability core material. The formula for inductance with a gapped core is:

$$L = \frac{(\mu)(A)(N^2)(0.4\pi)(10^{-8})}{\ell\left(1+\frac{\mu g}{\ell}\right)}$$

Inductance drops by the factor, $\left(1+\frac{\mu \bullet g}{\ell}\right)$

With a μ of 2000, ℓ = 2" and g = 0.02", inductance will drop by 22:1, requiring that N be increased by $\sqrt{22}$ to maintain constant inductance. Increase in energy storage is equal to the decrease in permeability.

$$\frac{E_{MAX}\ (\text{with gap})}{E_{MAX}\ (\text{no gap})} = 1+\frac{\mu \bullet g}{\ell}$$

There are several practical limits on the amount which gap size may be increased. First, large gaps require many more turns to achieve the same inductance. This requires smaller diameter wire which increases copper losses from I^2R heating. Secondly, with large gaps the *effective* gap size is considerably less than the actual gap because of fringing fields around the gap.

When using commercially available cores, data sheet information on ℓ, A and μ is usually given in *effective* values. The theoretical value of μ, for instance, is the bulk value for the core material. The *effective* value for a single piece core may approach the bulk value, but with 2-piece cores, the tiny air spaces left in the mating surfaces can reduce the *effective* permeability by as much as 2:1. This may sound unreasonably pessimistic, but a core with bulk μ = 3000 and ℓ = 1.5", will lose half its permeability for g = 0.0005". Data sheets for gapped cores list *effective* values of μ for each gap size to make calculations simple. They may also list a parameter, "inductance per (turn)^2" for each gap to further simplify inductance calculations.

There are two types of core material which are effectively self-gapped: iron powder and permalloy. These materials distribute the gap evenly throughout the core, allowing gapless core to be constructed with much higher energy storage capability. The permeability of this material is much reduced, but if the winding window will accommodate the extra turns, the current handling capability of the inductor will be much higher for the same inductance compared to a high-μ formulation.

Iron powder cores are cheaper than ferrite and can be custom tailored quickly, but high core loss limits their application to low AC flux density applications such as inductors. A significant advantage of iron powder is that it saturates very "softly," preventing catastrophic total loss of inductance for large overcurrent conditions. Note that commercially available powdered iron inductors are typically "optimized" so that core losses and winding (I^2R) losses are the same order of magnitude. Core loss is dependent on peak-to-peak ripple current which depends on the voltage-time product applied to the inductor. The inductors are therefore specified for a maximum DC current and a maximum volt•microsecond product to limit heating. For applications which require highest possible efficiency, consider using oversized cores or permalloy, which is more expensive, but has much lower core loss. Consult with inductor manufacturers about trading off DC current for ripple current, or vice versa.

Inductor Selection Process

The simplest way to select an inductor is to find an off-the-shelf unit that meets the minimum inductance and current

requirements. This may not be cost effective, however, if the standard types are not fairly close to your requirements. The next best approach is to have the unit custom wound by one of the many companies in the business. They will select the best core and winding combination for your particular application. A third approach is to scan the literature for standard core types which you can custom wind to meet your particular requirement. This is a quick way to get a prototype up and running. It can also be very cost effective for some production situations. At the end of this application note is a list of core and inductor/transformer manufacturers.

The procedure for selecting a do-it-yourself core starts with defining the values of peak winding current and inductance. If the LT1070 is to be used at or near full output power, peak winding current will approach 5A, so a conservative value of 5A should be used for core calculations. If external current limiting is used or if output power levels are lower, peak winding currents can be calculated from the equations supplied in the discussions of each topology. Likewise, inductance values are calculated from specific equations in these sections. Actual values for L generally fall into the range of 50µH to 1000µH, with 200µH to 500µH being most typical.

For ferrite cores, the next step is to calculate the core volume required to prevent saturation:

$$V_e = \frac{(I_P)^2(L)(\mu_e)(0.4\pi)}{(B_O)^2(10^{-8})} \quad \text{(ferrite cores)}$$

L = required inductance (henries)
I_P = peak inductor current (amps)
μ_e = effective relative permeability } supplied on core data sheets
B_O = maximum operating flux density (gauss) } supplied on core data sheets
V_e = effective core volume

Example: let L = 200µH, I_P = 5A, μ_e = 100, B_O = 2500 gauss,

$$V_e = \frac{(5)^2(200 \bullet 10^{-6})(100)(0.4\pi)}{(2500)^2(10^{-8})} = 10\text{cm}^3$$

The values chosen for μ_e and B_O are typical for a gapped ferrite core. Some cores come with several standard gaps.

Others are left ungapped with the user supplying spacers for setting gap length. Custom gapped cores are also available. A reasonable place to start is with a gap length of 0.02 inches. A core with μ = 3000 and path length (ℓ_e) of 2 inches would have an effective permeability of $\mu_e = \mu/(1 + \mu_g/\ell_e) = 3000/(1 + 3000 \bullet 0.02/2) = 97$. Notice that by simply selecting a large gap we can arbitrarily reduce the required core volume. The problem with attempting to use a large gap is that the effective permeability drops so low that a large number of turns are required to achieve the desired inductance. This forces the use of small diameter wire where the copper losses get high enough to cause overheating of the core.

Powdered iron cores, because of their high core loss and ability to operate at very high *DC* flux densities, generally have a different design procedure based on temperature rise due to core loss and winding loss. *AC* flux densities generally need to be kept below 400 gauss. This leads to a volume formula based on AC flux density:

$$V_C = \frac{(\Delta I)^2(L)(\mu)(0.4\pi)}{(4)(B_{AC})^2(10^{-8})}$$

ΔI = peak-to-peak ripple current

For ΔI = 1A, L = 200µH, μ = 75 and B_{AC} = 300 gauss,

$$V_C = \frac{(1)^2(200 \bullet 10^{-6})(75)(0.4\pi)}{(4)(300)^2(10^{-8})} = 5.25\text{cm}^3$$

To reduce core size, inductance (L) must be *increased*. This seems backwards according to the formula, but ΔI is inversely proportional to L, so the $(\Delta I)^2$ term drops rapidly as L is increased, reducing required core volume. The penalty is increased wire (copper) loss due to the increased turns required.

After a tentative core is selected based on volume, a check must be done to see if the power losses from the winding(s) and the core itself are within the allowed limits.

The first step is to calculate the number of turns required:

$$N = \sqrt{\frac{(L)(\ell_e)}{(\mu_e)(A_e)(0.4\pi \bullet 10^{-8})}}$$

N = turns
ℓ_e = effective magnetic path length (cm)
A_e = effective core area (cm^2)
μ_e = effective permeability (with gap)

} supplied on core data sheets

Using the ferrite example, and assigning ℓ_e = 9cm, A_e = 1.2cm^2, μ_e = 100, a 200µH inductor would require:

$$N = \sqrt{\frac{(200 \bullet 10^{-6})(9)}{(100)(1.2)(0.4\pi \bullet 10^{-8})}} = 34.6 \text{ turns (use 35)}$$

To calculate wire size, the usable winding window area (Aw) must be ascertained from the core dimensions. Many data sheets list this parameter directly. The usable window area must allow for bobbin thickness and clearances. Total copper area is only about 60% of window area due to air gaps around the wire. We can now express the required wire gauge in terms of N and Aw.

$$\text{Wire gauge (AWG)} = 10\left(\log\frac{(0.08)(N)}{(0.6)(Aw)}\right)$$

0.08 factor = area of #1 gauge wire
0.6 factor = air space loss around wire

If we assume a value for Aw of 0.2in^2 and use N = 35:

$$AWG = 10\log\frac{(0.08)(35)}{(0.6)(0.2)} = 13.68 \text{ (use \#14)}$$

The next step is to determine the number of winding layers. This is determined by bobbin length, or toroid inside circumference:

$$\text{Layers} = \frac{N(D+0.01)}{L_B} = \frac{N\left[(0.32)\left(10^{\frac{-AWG}{20}}\right)+0.01\right]}{L_B}$$

D = wire diameter in inches
L_B = bobbin length or toroid inside circumference
0.01 = allowance for enamel and spacing

For N = 35, AWG = #14 and L_B = 0.9":

$$\text{Layers} = \frac{35\left[(0.32)\left(10^{\frac{-14}{20}}\right)+0.01\right]}{0.9} = 2.87$$

The reason for calculating layers is that the *AC copper losses* are very dependent on the number of layers in a winding. To calculate AC losses, a table is used (Figure 48) which requires a factor K:

$$K = D\sqrt{(f)(F_P)}$$

D = wire diameter or foil thickness

For foil conductors, F_P is 1. For round wires it is equal to:

$$F_P = \frac{(T_L+1)(N_C)(D)}{L_W}$$

T_L = turns per layer
N_C = number of paralleled conductors (bifilar→N_C = 2)
D = wire diameter
L_W = length of winding (≈ L_B)

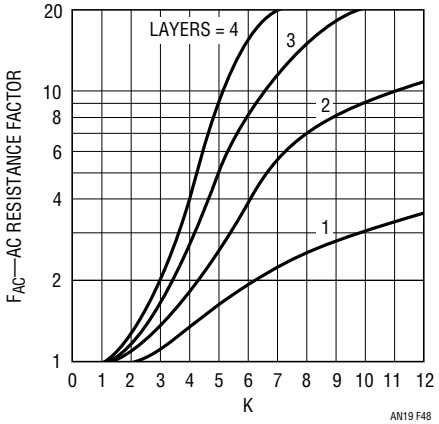


Figure 48. AC Resistance Factor

For 35 turns and 3 layers, $T_L \approx 12$. #14 wire has D = 0.064. N_C for a single wire is 1. With L_W = 0.9":

$$F_P = \frac{(12+1)(1)(0.064)}{0.9} = 0.92$$

K is now equal to:

$$K = D\sqrt{(f)(F_P)} = 0.064\sqrt{(40 \bullet 10^3)(0.92)} = 12.3$$

This is a very high K factor; in fact it is slightly off the graph in Figure 48, but for now it illustrates the importance of AC resistance calculations. The various lines on the graph represent the number of layers. With three layers, the AC resistance factor is off scale at approximately 23. This means that AC resistance is *23 times* DC resistance. Now we can calculate winding losses. DC winding resistance is found from:

$$R_{DC} = \frac{(N)(\ell_m)}{12}\left(10^{\frac{AWG}{10}-4}\right)$$

ℓ_m = mean turn length (core specification)

For N = 35, ℓ_m = 2.4", AWG = #14:

$$R_{DC} = \frac{(35)(2.4)}{12}\left(10^{\frac{AWG}{10}-4}\right) = 0.0176\Omega$$

AC resistance is then DC resistance multiplied by AC resistance factor (F_{AC}).

$R_{AC} = (R_{DC})(F_{AC}) = (0.0176)(23) = 0.404\Omega$

To calculate total losses, DC and AC losses are summed:

$P_W = (I_{DC})^2(R_{DC}) + (I_{AC})^2(R_{AC})$

Formulas for I_{DC} and I_{AC} are shown in Figure 50. If we assume I_{DC} = 5A and I_{AC} = 1A, total winding losses are:

$P_W = (5)^2(0.0176) + (1)^2(0.404) = 0.44 + 0.4 = 0.94W$

In this example, AC losses are about equal to DC losses. Simple inductors used in buck, boost and buck/boost designs may have the ratio of AC to DC losses in the range of 0.25 to 4.0. Transformer designs like flyback usually have AC losses *much* higher than DC losses. Losses in the primary and secondary are calculated separately. In many cases, multiple strands of smaller wire or copper foil must be used to reduce the AC resistance factor to acceptable limits.

After winding losses are found, core loss must be calculated. The first step is to find peak *AC* flux density:

$$B_{AC} = \frac{L(\Delta I)}{(2N)(A_e)(10^{-8})}$$

ΔI = peak-to-peak winding ripple current

ΔI is the *ripple* current in the winding. It is the *change* in winding current during the time current is flowing in the winding. For L = 200µH, ΔI = 2A, N = 35 and A_e = 1.2cm^2:

$$B_{AC} = \frac{(200 \bullet 10^{-6})(2)}{(35)(1.2)(10^{-8})} = 476 \text{ gauss}$$

Core loss *per unit volume* (F_{fe}) is found from the manufacturers tables (see Figure 49) of F_{fe} vs flux density and frequency or from the following formula for typical M_NZ_N ferrite material (ferroxcube type 3C8):

$F_{fe} = (1.3 – 10^{-14})(B_{AC})^2(f^{1.45})$

For B_{AC} = 476 gauss, f = 40kHz:

$F_{fe} = (1.3 \bullet 10^{-14})(476)^2(40 \bullet 10^3)^{1.45} = 0.014W/cm^3$

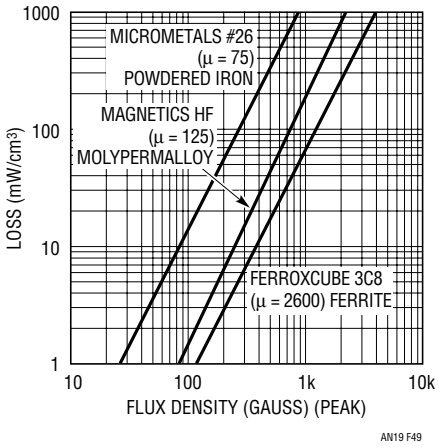


Figure 49. Core Loss vs Flux Density

Total core loss is F_{fe} times core volume:

$P_C = (F_{fe})(V_e) = (0.014)(10) = 0.14W$

V_e = effective core volume (cm^3)

Core loss for a powdered iron core is approximately 25 times higher than for ferrite. At a lower flux density of 150 gauss, a powdered iron core would still have core losses 2.5 times that of ferrite. Copper losses would also be higher because of the higher inductance required to reduce AC flux density. Powdered iron cores must be carefully designed to avoid overheating.

Overall losses in the ferrite core are the sum of winding losses plus core losses:

$P = P_W + P_C = 0.94 + 0.14 = 1.08W$

This loss reflects on regulator efficiency, and more importantly, core temperature rise. A $10cm^3$ core might have a typical thermal resistance of 20°C/W. Temperature rise in this core with P = 1.08W = (1.08)(20) = 21.6°C. 40°C rise is considered a typical design criterion, so this core is being under utilized.

Transformer Design Example

Requirements: A flyback converter with V_{IN} = 28V_{DC}, V_{OUT} = 5V, I_{OUT} = 6A. From previous calculations it is found that N = 1/3, L_{PRI} = 200µH and $I_{PRI(PEAK)}$ = 4.5A, with ΔI = 1A.

1. Calculate volume of core required with a gapped core. First assume an effective permeability of ≅150 and B_O = 2500 gauss:

$$V_e = \frac{(I_{PRI})^2(L)(\mu_e)(0.4\pi)}{(B_O)^2(10^{-8})}$$

$$= \frac{(4.5)^2(200 \bullet 10^{-6})(150)(0.4\pi)}{(2500)^2(10^{-8})} = 12cm^3$$

A Pulse Engineering core #0128.005 has $V_e = 13.3cm^3$, $A_e = 1.61cm^2$, $\ell_e = 8.26cm$, $\mu = 2000$.

2. Calculate required gap:

$$g = \frac{\ell_e\left(\frac{\mu}{\mu_e} - 1\right)}{\mu}$$

$$= \frac{8.26\left(\frac{2000}{150} - 1\right)}{2000} = 0.051cm = 0.02''$$

If an ungapped core is used with spacers, spacer thickness should be 0.02/2 = 0.01".

3. Calculate required turns:

$$N = \sqrt{\frac{(L)(\ell_e)}{(\mu_e)(A_e)(0.4\pi \bullet 10^{-8})}}$$

$$= \sqrt{\frac{(200 \bullet 10^{-6})(8.26)}{(150)(1.61)(0.4\pi \bullet 10^{-8})}} = 23.3$$

4. Calculate wire size. Allocate 1/2 the window space for the primary winding. Window height (build) for the 0128.005 core is 0.25" and coil length is 0.782", giving a window area = (0.25)(0.782) = $0.196in^2$:

$$AWG = 10 \log \frac{0.08N}{(0.6)(Aw)} = 10 \log \frac{(0.08)(23)}{(0.6)\left(\frac{0.196}{2}\right)}$$

$$= 14.95 \text{ (use \#16)}$$

5. Calculate layers:

$$\text{Layers} = \frac{N\left[(0.32)\left(10^{\frac{-AWG}{20}}\right) + 0.01\right]}{L_B}$$

$$= \frac{23\left[(0.32)\left(10^{\frac{-16}{20}}\right) + 0.01\right]}{0.782}$$

$$= 1.79 \text{ (assume 2 layers)}$$

6. Calculate K factor (#16 wire has D = 0.05):

$$F_P = \frac{(T_L + 1)(N_C)(D)}{L_W} = \frac{\left(\frac{23}{2} + 1\right)(1)(0.05)}{0.782} = 0.8$$

$$K = D\sqrt{(f)(F_P)} = 0.05\sqrt{(40 \bullet 10^3)(0.8)} = 8.94$$

7. Calculate DC winding resistance:

$$R_{DC} = \frac{(N)(\ell_m)}{12}\left(10^{\frac{AWG}{10}-4}\right) = \frac{(23)(3)\left(10^{\frac{16}{10}-4}\right)}{12} = 0.023\Omega$$

(ℓ_m for this core is $\approx$3")

8. Use graph to find AC resistance factor. Interleaving of primary and secondary reduces effective layers by two only if primary and secondary conduct simultaneously, which they *do not* in a flyback design. Use layers = 2 line:

   F_{AC} = 8.3 (from graph, for K = 8.95)

9. Calculate AC winding resistance:

   $R_{AC} = (R_{DC})(F_{AC}) = (0.023)(8.3) = 0.19\Omega$

10. Calculate primary winding losses.

    First, primary AC RMS current must be calculated. From the chart in Figure 50:

$$I_{AC} = \frac{I_{OUT}}{E}\sqrt{\frac{(N)(V_{OUT})}{V_{IN}}}$$

$$= \frac{6}{0.75}\sqrt{\frac{(1/3)(5)}{28}} = 1.95A$$

$$I_{DC} = \frac{I_{OUT}}{E}\sqrt{\frac{V_{OUT}(V_{OUT} + N \bullet V_{IN})}{(V_{IN})^2}}$$

$$= \frac{6}{0.75}\sqrt{\frac{5(5 + 1/3 \bullet 28)}{(28)^2}} = 2.4A$$

Power loss in the primary winding is:

$P_W = (I_{AC})^2 R_{AC} + (I_{DC})^2 R_{DC}$
$= (1.95)^2 (0.19) + (2.4)^2 (0.023) = 0.85W$

11. Calculate secondary winding loss.

    Turns ratio is 1/3, so the secondary will have 23/3 = 7.67 turns. Use 8 turns:

$$AWG = 10 \log\frac{0.08N}{0.6Aw} = 10 \log\frac{(0.08)(8)}{(0.6)\left(\frac{0.196}{2}\right)} = 10.4$$

This is rather large, stiff wire and the large diameter will lead to large AC winding losses. A good solution might be to use multiple smaller diameter wire wound in parallel. If we use the length of the coil divided by 2N, it will tell us what diameter wire can be bifilar wound to just fill one layer:

$$D = \frac{L_B}{2N} = \frac{0.782}{(2)(8)} = 0.049''$$

The next smallest standard wire diameter is #18. Two #18 wires have three times the DC resistance of a single #10 wire, but AC resistance will not increase nearly that much. Assume one layer bifilar wound #18 secondary interleaved between the two primary layers (to reduce leakage inductance).

$$R_{DC} = \frac{(N)(\ell_m)}{12}\left(10^{\frac{AWG}{10}-4}\right) = \frac{(8)(3)}{12}\left(10^{\frac{18}{10}-4}\right)$$

$= 0.013\Omega$ *per wire*

With two wires, total R_{DC} = 0.013/2 = 0.0065Ω.

$$F_P = \frac{(T_L + 1)(N_C)(D)}{L_W} = \frac{(8 + 1)(2)(0.04)}{0.782} = 0.92$$

$$K = D\sqrt{(f)(F_P)} = 0.04\sqrt{(40 \bullet 10^3)(0.92)} = 7.7$$

From graph, with layers = 1, F_{AC} = 2.3:

$R_{AC} = (R_{DC})(F_{AC}) = (0.0065)(2.3) = 0.015\Omega$

From the chart in Figure 50:

$$I_{AC} = I_{OUT}\sqrt{\frac{V_{OUT}}{N(V_{IN})}} = 6\sqrt{\frac{5}{1/3(28)}} = 4.4A$$

$$I_{DC} = I_{OUT}\sqrt{\frac{V_{OUT}+N(V_{IN})}{N(V_{IN})}} = 6\sqrt{\frac{5+1/3(28)}{1/3(28)}} = 7.4A$$

$P_W = (4.4)^2(0.015)+(7.4)^2(0.0065) = 0.65W$

12. Calculate core loss.

Core loss is proportional to *AC* flux density which is determined by *change* in primary current (ΔI) during primary current flow period. For ΔI = 1A:

$$B_{AC} = \frac{L(\Delta I)}{2(N)(A_e)(10^{-8})} = \frac{(200\bullet 10^{-6})(1)}{2(23)(1.61)(10^{-8})}$$

$= 270$ gauss

$$F_{fe} = (1.3\bullet 10^{-14})(B_{AC})^2(f^{1.45}) = 0.0045W/cm^3$$

$$P_C = (F_{fe})(V_e) = (0.0045)(13.3) = 0.06W$$

Total power loss with this core is:

$P = P_W + P_C = 0.85 + 0.65 + 0.06 = 1.56W$

The 0128.005 core is specified at 2.78W for a 40°C temperature rise, yielding θ = 40/2.78 = 14.4°C/W

$\Delta T(core) = (P)(\theta) = (1.56)(14.4) = 22°C$

TOPOLOGY	DC PRIMARY I	AC PRIMARY I	DC SECONDARY I	AC SECONDARY I
Flyback	$\frac{I_{OUT}}{E}\sqrt{\frac{V_{OUT}[V_{OUT}+N(V_{IN})]}{(V_{IN})^2}}$	$\frac{I_{OUT}}{E}\sqrt{\frac{N(V_{OUT})}{V_{IN}}}$	$I_{OUT}\sqrt{\frac{V_{OUT}+N(V_{IN})}{N(V_{IN})}}$	$I_{OUT}\sqrt{\frac{V_{OUT}}{N(V_{IN})}}$
Buck	I_{OUT}	(0.29)(ΔI)	NA	NA
Current-Boosted Buck	$I_{OUT}\sqrt{\frac{V_{OUT}[V_{OUT}+N(V_{IN}-V_{OUT})]}{(V_{IN})^2}}$	$I_{OUT}\sqrt{\frac{N[V_{OUT}(V_{IN}-V_{OUT})]}{(V_{IN})^2}}$	$I_{OUT}\sqrt{\frac{(V_{IN}-V_{OUT})[V_{OUT}+N(V_{IN}-V_{OUT})]}{N(V_{IN})^2}}$	$I_{OUT}\sqrt{\frac{V_{OUT}(V_{IN}-V_{OUT})}{N(V_{IN})^2}}$
Boost	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}}\right)$	(0.29)(ΔI)	NA	NA
Voltage-Boosted Boost	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}}\right)$	$(I_{OUT})(N)\sqrt{\frac{V_{OUT}-V_{IN}}{V_{IN}(N+1)}}$	$I_{OUT}\sqrt{\frac{V_{OUT}+N(V_{IN})}{V_{IN}(N+1)}}$	$I_{OUT}\sqrt{\frac{V_{OUT}-V_{IN}}{V_{IN}(N+1)}}$
Current-Boosted Boost	$I_{OUT}\sqrt{\frac{(V_{OUT}-V_{IN})[V_{OUT}+V_{IN}(N+1)]}{(V_{IN})^2}}$	$I_{OUT}\sqrt{\frac{N(V_{OUT}-V_{IN})}{V_{IN}}}$	$I_{OUT}\sqrt{\frac{V_{OUT}+V_{IN}(N+1)}{N(V_{IN})}}$	$I_{OUT}\sqrt{\frac{V_{OUT}-V_{IN}}{N(V_{IN})}}$
Buck-Boost (Inverting)	$I_{OUT}\left(1+\frac{V_{OUT}}{V_{IN}}\right)$	(0.29)(ΔI)	NA	NA
Forward	$I_{OUT}\sqrt{\frac{N(V_{OUT})}{V_{IN}}}$	$I_{OUT}\sqrt{\frac{V_{OUT}[N(V_{IN}-V_{OUT})]}{(V_{IN})^2}}$	$I_{OUT}\sqrt{\frac{V_{OUT}}{N(V_{IN})}}$	$I_{OUT}\sqrt{\frac{V_{OUT}[N(V_{IN}-V_{OUT})]}{N(V_{IN})^2}}$
'CUK	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}}\right)$	"0" or (0.29ΔI)	I_{OUT}	"0" or (0.29ΔI)

I_{OUT} = DC output current V_{OUT} = DC output voltage V_{IN} = DC input voltage

AN19 F50

Figure 50. AC and DC Winding Currents (RMS Equivalent)

This is a very conservative design. If minimum core size is required, the procedure now is to go back to step 1 and assume a lower effective permeability (μ_e), perhaps 100. This would reduce core volume and require a larger gap. More turns would be required and the available space for copper would go down, so copper losses would go up. Flux density remains constant, so core loss drops. Thermal resistance goes up however, so the smaller core gets hotter. In addition, the increased number of turns will increase leakage inductance, which will increase snubber losses. It isn't easy, folks!

HEAT SINKING INFORMATION

The efficiency of the LT1070 allows it to be used without a heat sink in many applications, but for full-power output a heat sink is required. The equations contained in the Efficiency section of this application note will allow the user to estimate fairly accurately the total power dissipation of the chip under full load conditions. Short-circuit power dissipation can be either *more or less* than full load, depending on the topology. Calculation of short-circuit power dissipation in the LT1070 is very complicated because the "on" time of the switch is strongly dependent on parasitic effects such as diode and inductor series resistance, wiring losses and leakage inductance. If continuous output shorts must be tolerated, it is strongly suggested that a temperature probe be used to ensure that maximum junction is not exceeded. Thermal resistance from junction to case is 2°C/W maximum, and short-circuit power dissipation almost never exceeds 10W, so a case temperature of 100°C for commercial units and 130°C for military units will ensure that maximum junction temperature is not exceeded.

Heat sink size for the LT1070 can be calculated if maximum power dissipation and maximum ambient temperature are known.

$$\theta_{HS} = \frac{T_J - T_A - (P)(\theta_{JC})}{P}$$

θ_{HS} = heat sink thermal resistance
P = LT1070 power dissipation
θ_{JC} = LT1070 junction-to-case thermal resistance (2°C/W)
T_J = LT1070 maximum junction temperature
T_A = maximum ambient temperature

For T_J = 100°C, T_A = 60°C, P = 5W:

$$\theta_{HS} = \frac{100 - 60 - (5)(2)}{5} = 6°C/W$$

TROUBLESHOOTING HINTS

The following is a list of "gotchas" we've put together to help you avoid some of the pitfalls of switching power supply design. They range from obvious to subtle and serious to hilarious. The LT1070 was specifically designed to eliminate many of the problems commonly found in power supply design and be easy to use. The problem is that there are a significant number of easily overlooked mistakes in breadboarding switching regulators which result in either instant death of the IC or electrical characteristics which are puzzling to even highly experienced power supply designers. So here's the list we've collected so far. We hope your problem is on it to save you time and frustration. If not, give us a call and we'll help fix the problem.

WARNING

Before reading this section, be aware that the intent of the author is not to insult, but rather to relate in an attention-getting manner a list of goofs that, in many cases, he personally has had to own up to.

1. **Transformer Wired Backwards**
   Those dots indicate polarity, not smashed flies.
2. **Electrolytic Capacitors Installed Backwards**
   This is no problem until you bend over to see what is wrong—then "bang," a personal demonstration of explosive venting.
3. **LT1070 Input and Switch Pins Reversed**
   The catalog and some preliminary data sheets got out with the wrong pinout for the plastic TO-220 package. Our apologies. *Pin 5 is input on TO-220 packages.*
4. **No Input Bypass Capacitor**
   Switching regulators draw current from the input supply in pulses. Long input wires can cause dips in

the input voltage at the switching frequency. *Breadboards should have a large (≥100µF) input capacitor up close to the regulator*.

5. Fred's Inductor (Or Transformer)

Inductors are not like lawn mowers. If you want to borrow the one out of Fred's drawer, make sure it's the right value for your application.

A 50µH inductor with 50V applied will have a current increasing with time at the rate of 1A per microsecond. It doesn't take a calculator to see that things can get out of hand quickly during the 25µs period of a 40kHz switcher. Likewise, if "Fred's inductor" is 50 *millihenries*, it will probably saturate at such low current levels that it is useless, not to mention the fact that the transient response can be measured on a Simpson VOM. *Use the formulas in the application note to get a ball park inductance value before starting a breadboard*.

6. Wimpy Magnetic Cores

Core sizes for the LT1070 will vary from $3cm^3$ to $20cm^3$ of core material for properly designed inductors or transformers. A thumbnail size core will simply saturate and get hot when asked to operate at ampere current levels. *Breadboard with man-sized cores, then optimize the core size for production*.

7. Rat's Nest Wiring

The LT1070 is not a jelly bean op amp that can be wired up with 2-foot clip leads. It achieves its high efficiency by switching current at very high speeds. Long wires will cause every component connected to them to look like an inductor at these speeds. This not only causes totally unpredictable operation; it can generate fatal (to components) transient voltages. *Use very short wires to interconnect power components on the breadboard, including bypass capacitors, catch diodes, LT1070 pins, transformer leads, etc*.

8. No Snubber Network

The LT1070 will tolerate a lot of abuse, but it cannot be overvoltaged on the switch pin and survive to tell the tale. The 65V maximum switch voltage must be observed. Any design using a transformer or tapped inductor will have enough leakage inductance to cause transients well above 65V if no snubber network is used. Load currents and input voltages should be increased slowly while monitoring switch voltage to ensure that the initial snubber design is adequate.

9. 60Hz Diodes

The LT1070 will *eat* 1N914 and 1N4001 diodes and not even burp. Diode currents, especially during start-up, can exceed 5A. This takes care of the 1N914s. The 1N4001s will last for a little while, until the heat generated by their horribly slow turn-off characteristics causes them to self-destruct. *Use diodes designed for switching applications, with adequate current ratings. Turn-on time is also important to avoid overvoltage stress on other components* (see Diode section).

10. Something from Nothing

The *first* step in designing with the LT1070 is to see if it will provide the required power level. Each topology has a different maximum output power that it can provide, depending on things such as input voltage, output voltage and transformer turns ratio. Secondary effects such as inductance values and switch resistance may also limit power. *The power graph on the next page is a rough guide to maximum power levels. Use it as a quick guide only*. More exact formulas are contained in the application section. Oh, by the way, if you thought about paralleling LT1070s for more power—sorry, it won't work. You cannot get to the internal 40kHz oscillator to get them in sync.

11. Input Supply Gets Clobbered

The LT1070 can draw input currents of up to 6A during start-up. It has to charge up the large output capacitor and it does this at a rate set by the internal current limit unless optional soft start is added. *The start-up surge may trip overcurrent latches on some supplies, causing them to stay off until power is recycled*.

Steady-state problems can also occur. Switching regulators try to deliver constant load voltage. With a given load, this means constant load power. For a high efficiency system, input power also remains constant, *so input current increases as input voltage decreases. Low input voltage conditions may require such high input currents that the input supply current limits. This*

causes the supply voltage to drop further, forcing a permanent latch condition. See current limit and soft start sections.

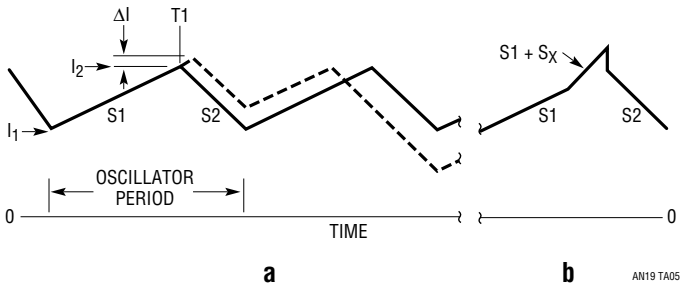
12. Didn't Read the Data Sheet
Then you shall have no pie.

13. Stray Coupling to the V_C or F_B Pins
Voltages on the FB and V_C pins are referenced to the LT1070 ground pin. In some topologies the ground pin is switching between input voltage and system ground. *Stray capacitance between V_C or FB pins and system ground* will act like coupling to a switching source. *Minimize this capacitance*. The problem is particularly acute when using an RC box to iterate frequency compensation on the V_C pin. Even configurations which have the LT1070 ground pin "grounded" may have problems if the RC box picks up switching energy.

SUBHARMONIC OSCILLATIONS

Current mode switching regulators which operate with a duty cycle greater than 50% and have continuous inductor current can exhibit a duty cycle instability known as subharmonic oscillations. This effect is not harmful to the regulator and in many cases it does not even affect the output regulation. Its most annoying effect is to produce a high pitched squeal from power components which effectively have their 40kHz operating frequency *modulated* by submultiple frequencies; 20kHz, 10kHz, etc. Subharmonic oscillations do *not* depend on the closed-loop characteristics of the regulator. They can occur even when zero feedback is used. Ordinary closed-loop instabilities can also cause audible sounds from switching regulators, but they tend to be in the range of hundreds of hertz to several kilohertz.

The source of subharmonic oscillations is the simultaneous conditions of fixed frequency and fixed peak amplitude of inductor current as shown in part a of the accompanying figure.



The inductor current starts at I_1, at the beginning of each switch on cycle. Current increases at a rate (S1) equal to input voltage divided by inductor value. When current reaches the trip level, I_2, the current mode loop shuts off the switch and current begins to fall at a rate S2 until the switch is again turned on by the oscillator. Now watch what happens when the point T1 is perturbed so that the current exceeds I_2 by ΔI. The time left for the current to fall is *reduced* so that the *minimum* current point is *increased* by $\Delta I + \Delta I S2/S1$. This will cause the minimum current on the *next* cycle to *decrease* by $(\Delta I + \Delta I\ S2/S1)(S2/S1)$. On each succeeding cycle the current perturbation is multiplied by S2/S1. If S2/S1 is greater than 1, the system is unstable. The condition $S2/S1 \geq 1$ occurs at a duty cycle of 50% or higher.

Subharmonic oscillations can be eliminated if an artificial ramp is superimposed on the inductor current waveform as shown in part b of the figure. If this ramp has a slope of S_X, the requirement for stability is that $S_X + S1$ be larger than S2. This leads to the following equation:

$$S_X \geq \frac{S1(2DC-1)}{1-DC}$$

DC = duty cycle

For duty cycles less than 50% (DC = 0.5), S_X is a negative number and is not required. For larger duty cycles, S_X takes on values dependent on S1 and duty cycle. S1 is simply V_{IN}/L. This yields an equation for the minimum value of inductance for a fixed value of S_X:

$$L_{MIN} \geq \frac{V_{IN}(2DC-1)}{S_X(1-DC)}$$

The LT1070 has an internal S_X *voltage* ramp fed into the current amplifier whose equivalent current referred value is 2 (10^5A/sec). A sample calculation for minimum inductance with V_{IN} = 15V, DC = 60% is shown:

$$L_{MIN} = \frac{(15)(2 \bullet 0.6-1)}{(2 \bullet 10^5)(1-0.6)} = 37.5\mu H$$

Remember that *for discontinuous operation, no subharmonic oscillations can occur. Likewise, with duty cycle less than 50%, there is no restriction on inductor size.*

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
- LT1070/LT1071 (Note 2) 40V
- LT1070HV/LT1071HV (Note 2) 60V

Switch Output Voltage
- LT1070/LT1071 ..... 65V
- LT1070HV/LT1071HV 75V

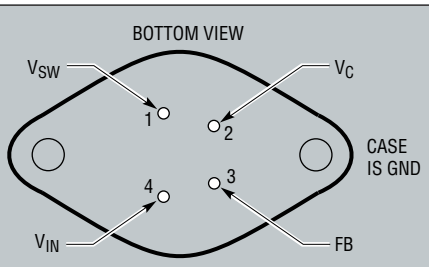
Feedback Pin Voltage (Transient, 1ms) ..... ±15V

Operating Junction Temperature Range
- Commercial (Operating) ..... 0°C to 100°C
- Commercial (Short Circuit) ..... 0°C to 125°C
- Industrial ..... –40°C to 125°C
- Military ..... –55°C to 150°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

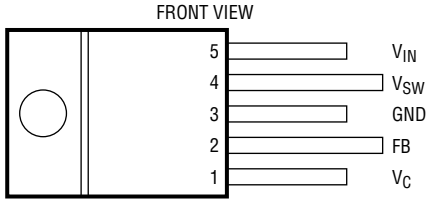


K PACKAGE
4-LEAD TO-3 METAL CAN

T_{JMAX} = 100°C, θ_{JA} = 35°C/W, Q_{JC} = 2°C (LT1070C, I)
T_{JMAX} = 150°C, θ_{JA} = 35°C/W, Q_{JC} = 2°C (LT1070M)
T_{JMAX} = 100°C, θ_{JA} = 35°C/W, Q_{JC} = 4°C (LT1071C, I)
T_{JMAX} = 150°C, θ_{JA} = 35°C/W, Q_{JC} = 4°C (LT1071M)

OBSOLETE PACKAGE

ORDER PART NUMBER
LT1070CK
LT1070HVCK
LT1070HVMK
LT1070IK
LT1070MK
LT1071CK
LT1071HVCK
LT1071HVMK
LT1071MK



T PACKAGE
5-LEAD PLASTIC TO-220

T_{JMAX} = 100°C, θ_{JA} = 75°C/W, Q_{JC} = 2°C (LT1070C, I)
T_{JMAX} = 100°C, θ_{JA} = 75°C/W, Q_{JC} = 4°C (LT1071C)

ORDER PART NUMBER
LT1070CT
LT1070HVCT
LT1070HVIT
LT1070IT
LT1071CT
LT1071HVCT
LT1071HVIT
LT1071IT

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin, V_C = 0.8V	 ●	1.224 1.214	1.244 1.244	1.264 1.274	V V
I_B	Feedback Input Current	V_{FB} = V_{REF}	 ●		350	750 1100	nA nA
g_m	Error Amplifier Transconductance	ΔI_C = ±25µA	 ●	3000 2400	4400	6000 7000	µmho µmho
	Error Amplifier Source or Sink Current	V_C = 1.5V	 ●	150 120	200	350 400	µA µA
	Error Amplifier Clamp Voltage	Hi Clamp, V_{FB} = 1V Lo Clamp, V_{FB} = 1.5V		1.80 0.25	 0.38	2.30 0.52	V V
	Reference Voltage Line Regulation	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.8V	●			0.03	%/V
A_V	Error Amplifier Voltage Gain	0.9V ≤ V_C ≤ 1.4V		500	800		V/V
	Minimum Input Voltage		●		2.6	3.0	V
I_Q	Supply Current	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.6V			6	9	mA
	Control Pin Threshold	Duty Cycle = 0	 ●	0.8 0.6	0.9	1.08 1.25	V V
	Normal/Flyback Threshold on Feedback Pin			0.4	0.45	0.54	V

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FB}	Flyback Reference Voltage	I_{FB} = 50µA		15	16.3	17.6	V
			●	14		18.0	V
	Change in Flyback Reference Voltage	0.05 ≤ I_{FB} ≤ 1mA		4.5	6.8	8.5	V
	Flyback Reference Voltage Line Regulation	I_{FB} = 50µA, 3V ≤ V_{IN} ≤ V_{MAX} (Note 3)			0.01	0.03	%/V
	Flyback Amplifier Transconductance (g_m)	ΔI_C = ±10µA		150	300	650	µmho
	Flyback Amplifier Source and Sink Current	V_C = 0.6V, I_{FB} = 50µA (Source)	●	15	32	70	µA
		V_C = 0.6V, I_{FB} = 50µA (Sink)	●	25	40	70	µA
B_V	Output Switch Breakdown Voltage	3V ≤ V_{IN} ≤ V_{MAX}, I_{SW} = 1.5mA					
		(LT1070/LT1071)	●	65	90		V
		(LT1070HV/LT1071HV)	●	75	90		V
V_{SAT}	Output Switch "On" Resistance (Note 4)	LT1070	●		0.15	0.24	Ω
		LT1071	●		0.30	0.50	Ω
	Control Voltage to Switch Current Transconductance	LT1070			8		A/V
		LT1071			4		A/V
I_{LIM}	Switch Current Limit (LT1070)	Duty Cycle ≤ 50%, T_J ≥ 25°C	●	5		10	A
		Duty Cycle ≤ 50%, T_J < 25°C	●	5		11	A
		Duty Cycle = 80% (Note 5)	●	4		10	A
	Switch Current Limit (LT1071)	Duty Cycle ≤ 50%, T_J ≥ 25°C	●	2.5		5.0	A
		Duty Cycle ≤ 50%, T_J < 25°C	●	2.5		5.5	A
		Duty Cycle = 80% (Note 5)	●	2.0		5.0	A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch "On" Time				25	35	mA/A
f	Switching Frequency			35	40	45	kHz
			●	33		47	kHz
DC (Max)	Maximum Switch Duty Cycle			90	92	97	%
	Flyback Sense Delay Time				1.5		µs
	Shutdown Mode Supply Current	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.05V			100	250	µA
	Shutdown Mode Threshold Voltage	3V ≤ V_{IN} ≤ V_{MAX}		100	150	250	mV
			●	50		300	mV

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Minimum switch "on" time for the LT1070/LT1071 in current limit is ≈1µs. This limits the maximum input voltage during short-circuit conditions, *in the buck and inverting modes only*, to ≈35V. Normal (unshorted) conditions are not affected. Mask changes are being implemented which will reduce minimum "on" time to ≤1µs, increasing maximum short-circuit input voltage above 40V. If the present LT1070/LT1071 (contact factory for package date code) is being operated in the buck or inverting mode at high input voltages and short-circuit conditions are expected, a resistor must be placed in series with the inductor, as follows:

The value of the resistor is given by:

$$R = \frac{t \bullet f \bullet V_{IN} - V_F}{I_{LIMIT}} - R_L$$

t = Minimum "on" time of LT1070/LT1071 in current limit, ≈1µs
f = Operating frequency (40kHz)
V_F = Forward voltage of external catch diode at I_{LIMIT}
I_{LIMIT} = Current limit of LT1070 (≈8A), LT1071 (≈4A)
R_L = Internal series resistance of inductor

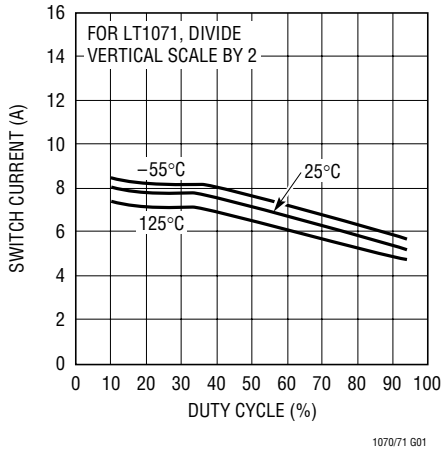
Note 3: V_{MAX} = 55V for LT1070HV and LT1071HV to avoid switch breakdown.

Note 4: Measured with V_C in hi clamp, V_{FB} = 0.8V. I_{SW} = 4A for LT1070 and 2A for LT1071.

Note 5: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by I_{LIM} = 3.33 (2 – DC) for the LT1070 and I_{LIM} = 1.67 (2 – DC) for the LT1071.

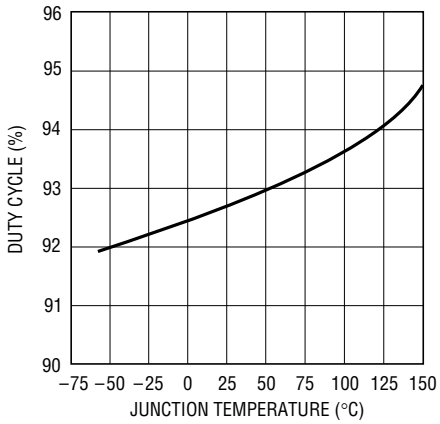
TYPICAL PERFORMANCE CHARACTERISTICS

Switch Current Limit vs Duty Cycle



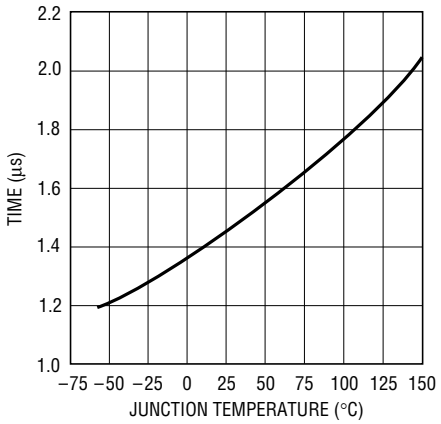
1070/71 G01

Maximum Duty Cycle



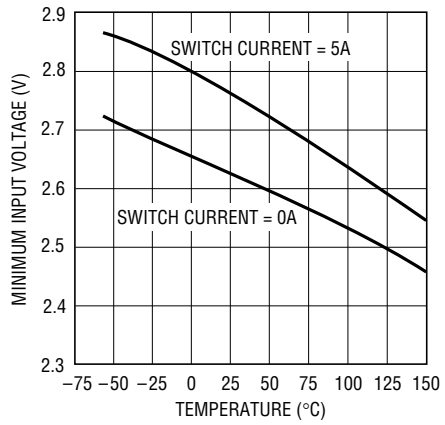
1070/71 G02

Flyback Blanking Time



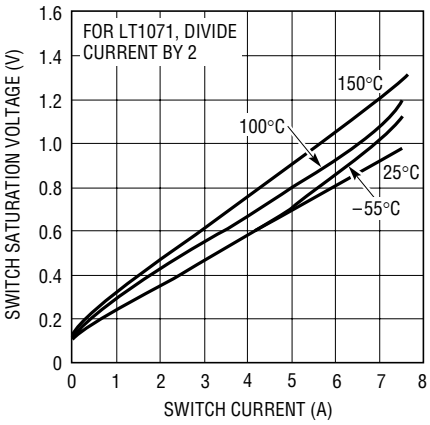
1070/71 G03

Minimum Input Voltage



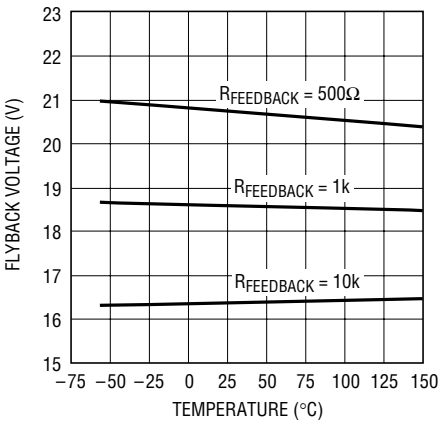
1070/71 G04

Switch Saturation Voltage



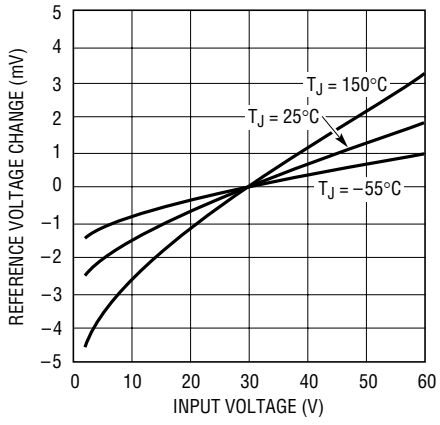
1070/71 G05

Isolated Mode Flyback Reference Voltage



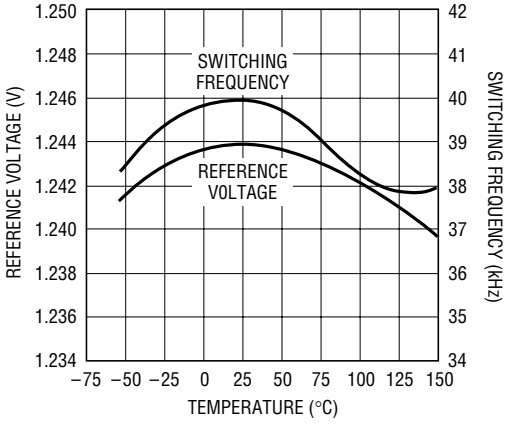
1070/71 G06

Line Regulation



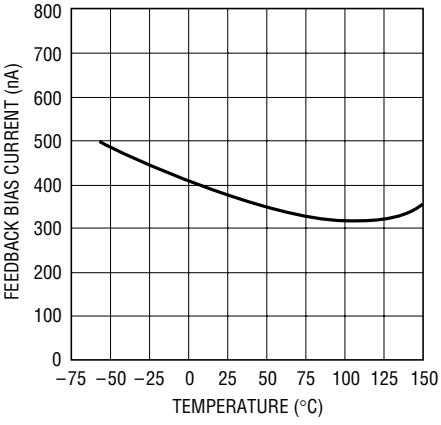
1070/71 G07

Reference Voltage vs Temperature



1070/71 G08

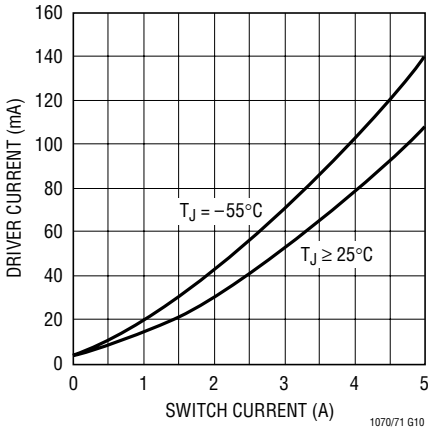
Feedback Bias Current vs Temperature



1070/71 G09

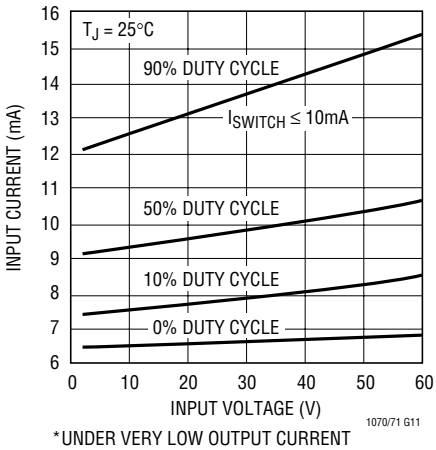
TYPICAL PERFORMANCE CHARACTERISTICS

Driver Current* vs Switch Current



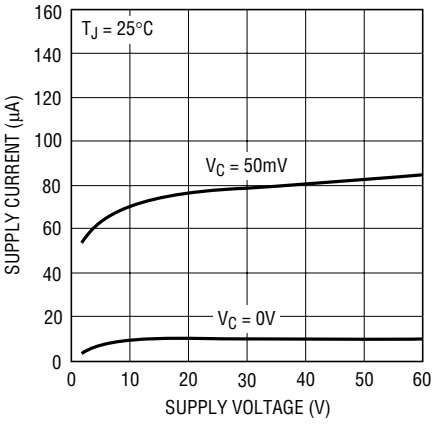
*AVERAGE LT1070 POWER SUPPLY CURRENT IS FOUND BY MULTIPLYING DRIVER CURRENT BY DUTY CYCLE, THEN ADDING QUIESCENT CURRENT

Supply Current vs Input Voltage*

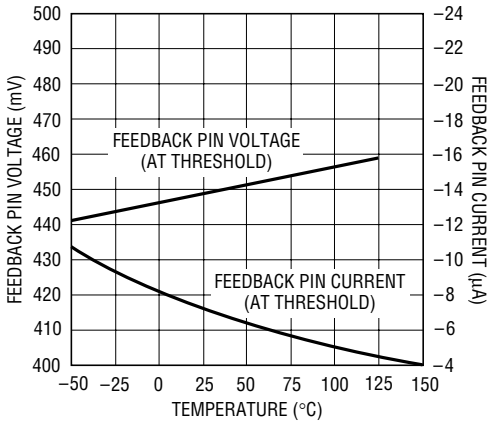


*UNDER VERY LOW OUTPUT CURRENT CONDITIONS, DUTY CYCLE FOR MOST CIRCUITS WILL APPROACH 10% OR LESS

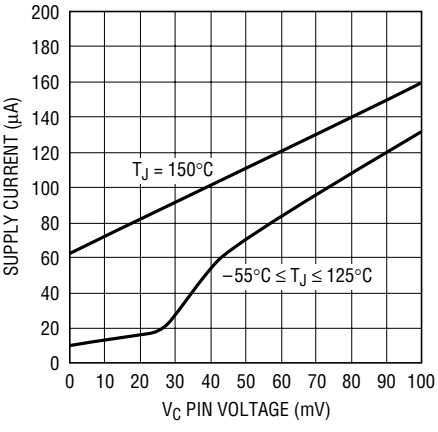
Supply Current vs Supply Voltage (Shutdown Mode)



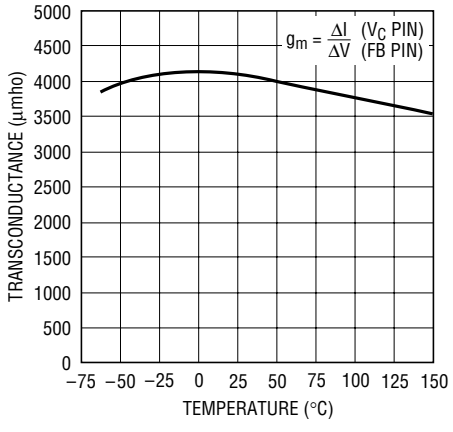
Normal/Flyback Mode Threshold on Feedback Pin



Shutdown Mode Supply Current

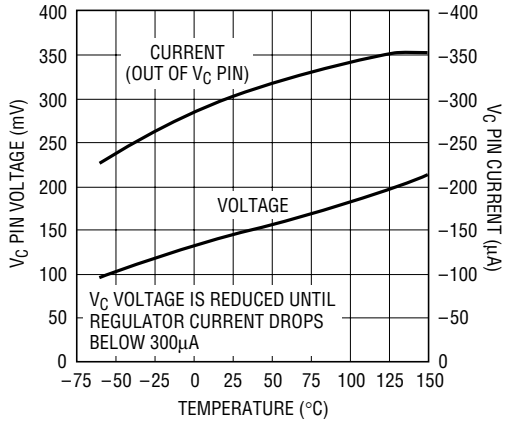


Error Amplifier Transconductance

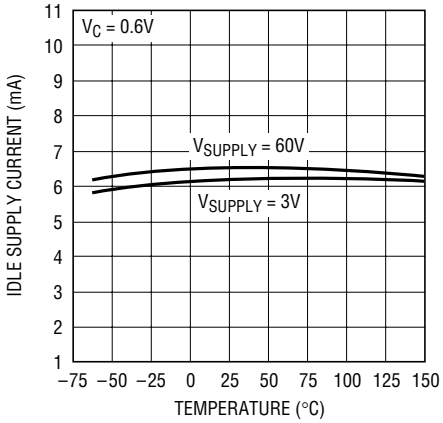


TYPICAL PERFORMANCE CHARACTERISTICS

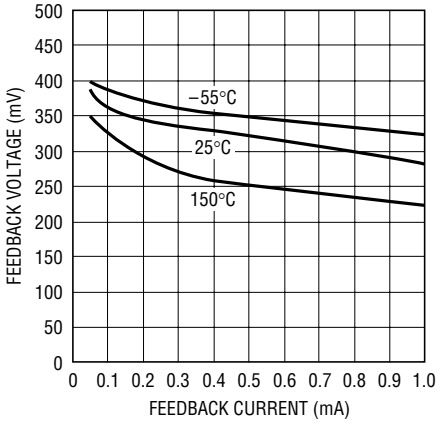
Shutdown Thresholds



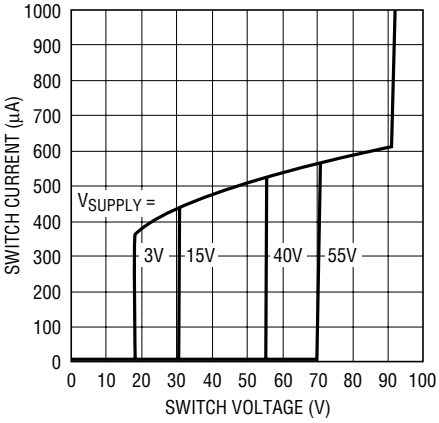
Idle Supply Current vs Temperature



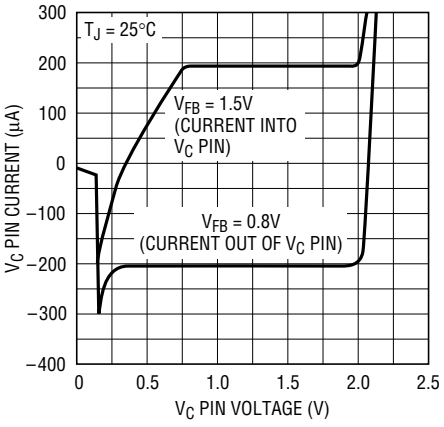
Feedback Pin Clamp Voltage



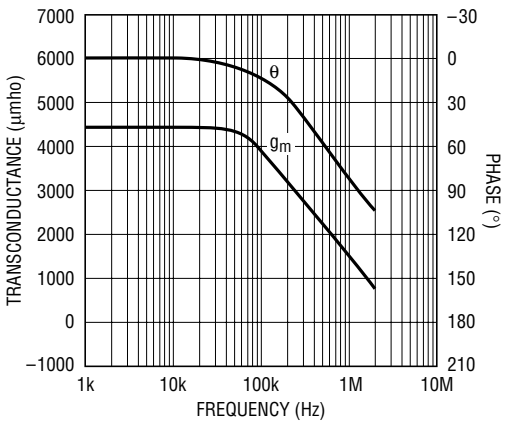
Switch "Off" Characteristics



V_C Pin Characteristics



Transconductance of Error Amplifier



INDUCTOR/TRANSFORMER MANUFACTURERS

Pulse Engineering Inc. (619/268-2400)
P.O. Box 12235, San Diego, CA 92112

Hurricane Electronics Lab (801/635-2003)
P.O. Box 1280, Hurricane, UT 84737

Coilcraft Inc. (312/639-2361)
1102 Silver Lake Rd., Cary, IL 60013

Renco Electronics, Inc. (516/586-5566)
60 Jefryn Blvd. East, Deer Park, NY 11729

CORE MANUFACTURERS

Ferroxcube (ferrites) (914/246-2811)
5083 Kings Highway, Saugerties, NY 12477

Micrometals (powdered iron) (714/630-7420)
1190 N. Hawk Circle, Anaheim, CA 92807

Pyroferric International Inc. (powdered iron)
(217/849-3300)
200G Madison St., Toledo, IL 62468

Fair-Rite Products Corp. (ferrites) (914/895-2055)
P.O. Box J, Wallkill, NY 12589

Stackpole Corp., Ferrite Products Group (814/781-1234)
Stackpole St., St. Mary's, PA 15857

Magnetics Division–Spang & Co.(ferrites)(412/282-8282)
P.O. Box 391, Butler, PA 16003

TDK Corp. of America, Industrial Ferrite Products
(312/679-8200)
4709 W. Golf Rd., Skokie, IL 60076

BIBLIOGRAPHY

Pressman, A.I., "Switching and Linear Power Supply, Power Converter Design," Hayden Book Co., Hasbrouck Heights, New Jersey, 1977, ISBN 0-8104-5847-0.

Chryssis, G., "High Frequency Switching Power Supplies, Theory and Design," McGraw Hill, New York, 1984, ISBN 0-07-010949-4.

Grossner, N.R., "Transformers for Electronic Circuits," McGraw Hill, New York, 1983, ISBN 0-07-024979-2.

Middlebrook, R.D., and 'Cuk, S., "Advances in Switched Mode Power Conversion," Volumes I, II, III, TESLA Co., Pasadena, CA, 1983.

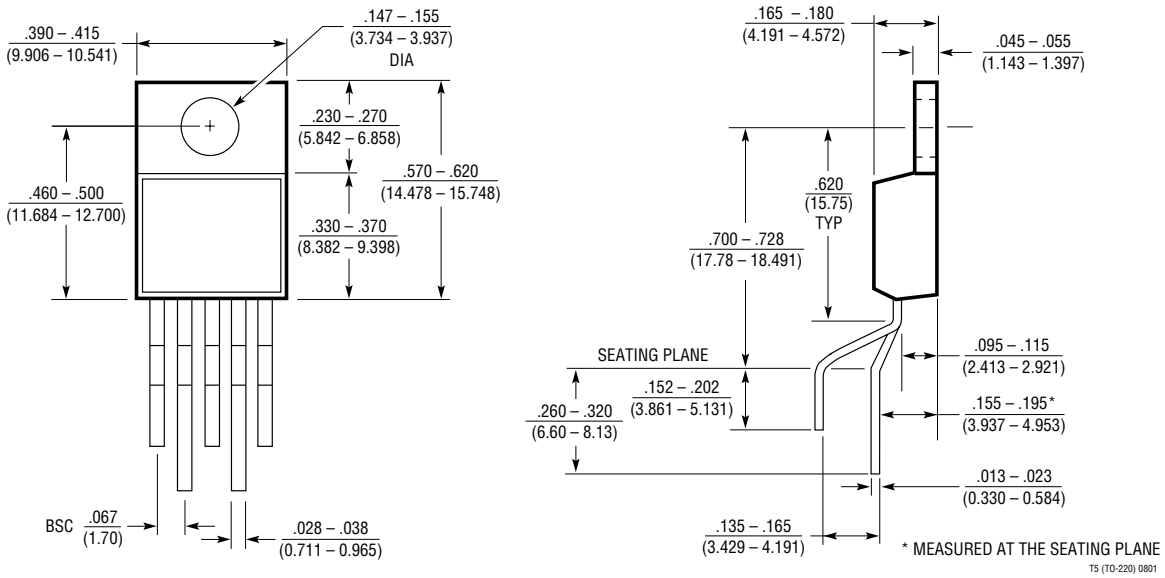
Proceedings of Powercon, Power Concepts, Inc.
Box 5226, Ventura, CA

"Linear Ferrite Magnetic Design Manual,"
Ferroxcube Inc., Saugerties, NY

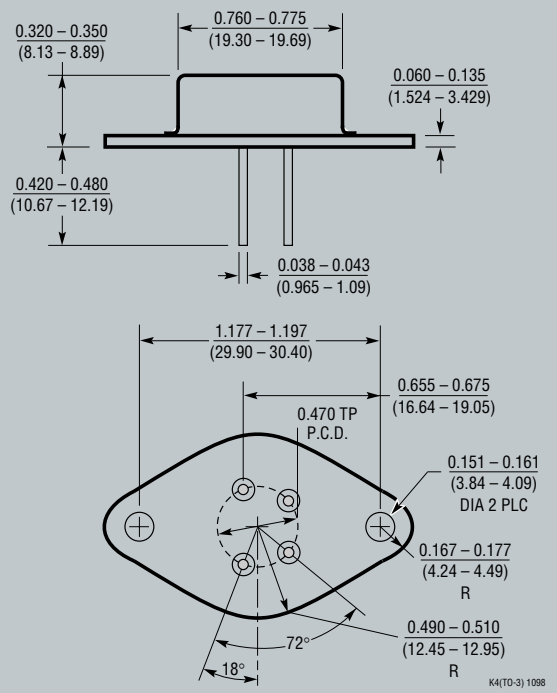
"Design Manual for SMPS Power Transformers,"
Pulse Engineering Inc., San Diego, CA

PACKAGE DESCRIPTION

T Package
5-Lead Plastic TO-220 (Standard)
(LTC DWG # 05-08-1421)



K Package
4-Lead TO-3 Metal Can
(LTC DWG # 05-08-1311)



OBSOLETE PACKAGE

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
LT 0206 REV B • PRINTED IN USA